Design and Linearization of Class-E Power Amplifier for Nonconstant Envelope Modulation

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***Abstract*—This paper presents design and linearization techniques for a highly efficient, but nonlinear Class-E power amplifier (PA) applied to linear RF transmitters. To achieve maximum efficiency for Class-E PA operating above gigahertz frequencies, the proposed design theory modifies the classic Class-E condition and considers switch-on and switch-off resistances in deriving the analytical solution. For linearization, a digital envelope predistorter (DEP) is used to provide predistorted envelope modulation for the RF-input and supply-voltage signals fed to the Class-E PA. This DEP can successfully compensate for AM/AM and AM/PM distortions such that the Class-E PA, although classified as a switching-mode PA, can act as a linear PA. A cdma2000 1 × transmitter incorporating this Class-E PA and DEP is demonstrated to simultaneously achieve high efficiency and high modulation quality.**

***Index Terms*—cdma2000 1 × transmitter, class-E power amplifier (PA), digital predistorter, PA linearization techniques.**

I. Introduction

As THE demand of video and data transmission increases, modern mobile communication standards often adopt more progressive modulation schemes, such as quadrature phase-shift keying (QPSK), quadrature amplitude modulation (QAM), or orthogonal frequency division multiplexing (OFDM), to accommodate high data-rate requirements. These modulation schemes are classified into the nonconstant envelope modulation scheme and require a linear power amplifier (PA) to transmit the modulated RF signal. However, there is an inherent tradeoff between linearity and efficiency in linear PA design. Generally speaking, power backoff is the most common approach used to prevent the nonlinear effects of linear PAs. The output power of PA backs off from the 1-dB compression point until the output signal quality satisfies the system requirement. For a high peak-to-average power ratio (PAPR) system, the power backoff value must be increased accordingly to avoid signal distortion. Unfortunately, the PA's efficiency peaks only when the PA operates near saturation and drops rapidly as the output power decreases.

Linear transmitters using nonlinear PAs, such as the linear amplification with nonlinear components (LINC) [1]–[3], envelope elimination and restoration (EER) [4], [5], and polar modulation [6]–[8] architectures, have received great attention for application in mobile communication systems because they can operate with high efficiency and high linearity. Thanks to the design simplicity in load network and high-efficiency switching operation, Class-E PAs were most often seen in the EER and polar modulation architectures. The Class-E PA was first introduced and analyzed by Sokal and Sokal in an equivalent simplified circuit with an ideal switch and an infinite dc-feed inductance [9]. Zulinski and Steadman found the design solution for a Class-E amplifier with finite dc-feed inductance [10]. Avratoglou *et al.* solved the problem using Laplace transforms for Class-E amplifiers having an arbitrary Q factor output load network [11]. Kazimierczuk and Puczko [12] and Klehn and Islam [13] considered finite dc-feed inductance and switch current fall time. Mandojana *et al.* performed a discrete time-domain analysis of a Class-E amplifier with switch-on and off resistances [14]. All the methods mentioned above require iterative or recursive approaches.

To directly evaluate the element values from given circuit specifications, Acar *et al.* proposed an analytical method to find exact design solutions for Class-E PA with finite dc-feed inductance [15]. Li and Yam also developed analytical solutions, which considered finite dc-feed inductance [16] or switch-on resistance [17]. Gaudo [18] and Mury and Fusco [19] provided a Class-E PA analytical method that considers both switch-on resistance and finite dc-feed inductance. In [20]–[24], the authors derived analytical solution that further includes package bondwire inductance. Nevertheless, the experimental results for RF Class-E PAs at gigahertz and sub-gigahertz frequencies often showed that one cannot simply rely on the previously published analytical design equations for the best efficiency design, as was discussed by Lie *et al.* [25]. In the research, the authors found that the high-frequency loss issues would be the main cause because the classic Class-E condition used in these previous Class-E PA designs is true for maximum efficiency based on a lossless switching device model. To overcome the problems, this paper provides a more complete analytical solution based on [20]–[24]. The theory presented differs from the previous ones in [20]–[24] in two aspects, which are: 1) the switch-off resistance effects are included and 2) the classic Class-E condition is modified to find maximum efficiency with considering the

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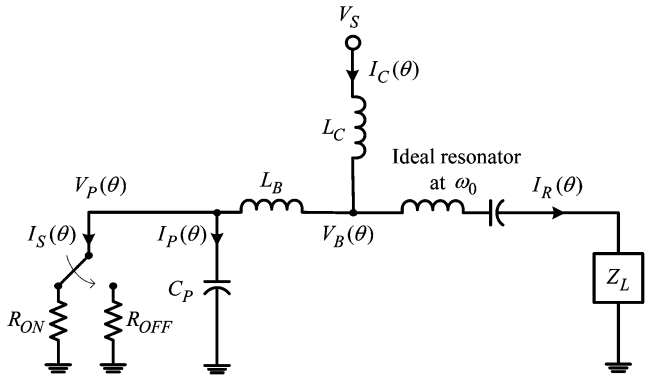

Fig. 1. Simplified equivalent circuit of a Class-E PA.

losses in a switching device model. With the help of this theory, the authors accomplish a new Class-E PA design with results showing very good agreement between theory and experiment.

In the aspect of linearization, EER and polar modulation techniques provide an effective way to linearize Class-E PAs for application to linear RF transmitters. However, their drawbacks include requiring wide envelope signal processing bandwidth and degrading efficiency under power backoff. In contrast, the hybrid quadrature polar modulation (HQPM) technique proposed by the authors in [20]–[24] can alleviate these drawbacks of EER and polar modulation techniques in the linearization of Class-E PAs. The HQPM technique has its own disadvantage. It encounters an obvious nonlinear characteristic at low signal amplitude, which counts on a digital predistorter to compensate for the nonlinear effects. It is noted that the digital predistorters used in [20]–[24] compensate for only AM/AM distortion. The digital predistorter used in this work can additionally compensate for AM/PM distortion, and thus, leads to better improvement in output signal quality.

II. Design Theory

Fig. 1 illustrates a simplified equivalent circuit of a Class-E PA, which treats a power transistor as an on-and-off switch. The classic Class-E condition enforces that the transistor output voltage and its differentiation must vanish at the transition from switch-off to switch-on to achieve maximum dc-to-RF efficiency. This condition can ideally lead to 100% dc-to-RF efficiency for a lossless switch, but for a switch that considers switch-on resistance $(R_{\rm ON})$ and switch-off resistance $(R_{\rm OFF})$ to practically account for transistor losses, this Class-E condition may not lead to the maximum dc-to-RF efficiency. In another consideration, to achieve the maximum dc-to-RF efficiency, all the reactive elements and the load network impedance shown in Fig. 1 must be carefully designed to have minimum overlap between switching voltage (V_P) and current (I_S) waveform at the designated operating frequency and output power. However, the transistor output capacitance (C_P) constructs a minimum parallel reactance at the output load network and limits the highest operating frequency to satisfy the maximum efficiency condition. To increase the highest operating frequency, the dc-feed choke can be replaced with a finite-valued inductor. The finite dc-feed inductance (L_C) is, in effect, approximately in parallel with output capacitance, and can be regarded as reducing the amount of output capacitance. To use a packaged transistor in the Class-E PA, the package bond-wire inductance (L_B) will play another important role in affecting the output capacitance effects.

Assume that the output current contains only fundamental components. It can be represented by a sinusoidal waveform given as

$$I_R(\theta) = I_O \sin(\theta + \phi) \tag{1}$$

where $\theta = \omega_0 t$. The amplitude of sinusoidal current (I_O) and the phase shift (ϕ) are to be determined. The switching voltage can be derived as

$$V_P(\theta) = V_B(\theta) - \omega L_B \frac{d}{d\theta}[I_C(\theta) - I_O \sin(\theta + \phi)] \tag{2}$$

where

$$V_B(\theta) = V_S - \omega L_C \frac{d}{d\theta} I_C(\theta). \tag{3}$$

Current flows through the output capacitance can be formulated as

$$\begin{aligned} I_P(\theta) &= \omega C_P \frac{d}{d\theta} V_P(\theta) \\ &= -\omega^2 C_P L_T \frac{d^2}{d\theta^2} I_C(\theta) - \omega^2 C_P L_B I_O \sin(\theta + \phi) \end{aligned} \tag{4}$$

where $L_T = L_B + L_C$. Current flows through the switch can be found as

$$\begin{aligned} I_S(\theta) &= \frac{V_P(\theta)}{R_{SW}(\theta)} \\ &= \frac{V_S}{R_{SW}(\theta)} - \frac{\omega L_T}{R_{SW}(\theta)} \frac{d}{d\theta} I_C(\theta) \\ &\quad + \frac{\omega L_B}{R_{SW}(\theta)} I_O \cos(\theta + \phi) \end{aligned} \tag{5}$$

where

$$R_{SW}(\theta) = \begin{cases} R_{\rm ON}, & 0 < \theta \le \pi \\ R_{\rm OFF}, & \pi < \theta \le 2\pi. \end{cases} \tag{6}$$

Note that the transistor conducts and cuts off when $0 < \theta \le \pi$ and $\pi < \theta \le 2\pi$, respectively. From Kirchoff's current law (KCL), all the currents expressed above must obey the following relation:

$$I_R(\theta) + I_P(\theta) + I_S(\theta) = I_C(\theta). \tag{7}$$

Substituting (1), (4), and (5) into (7) yields a second-order inhomogeneous ordinary differential equation for I_C, which is given as

$$\begin{aligned} &\omega^2 C_P L_T \frac{d^2}{d\theta^2} I_C(\theta) + \frac{\omega L_T}{R_{SW}(\theta)} \frac{d}{d\theta} I_C(\theta) + I_C(\theta) \\ &\quad = \frac{V_S}{R_{SW}(\theta)} + \left(1 - \omega^2 C_P L_B\right) I_O \sin(\theta + \phi) \\ &\qquad + \frac{\omega L_B}{R_{SW}(\theta)} I_O \cos(\theta + \phi). \end{aligned} \tag{8}$$

Solving for (8) yields the following general solution:

$$\begin{aligned} I_{C,\mathrm{ON,OFF}}(\theta) &= A_{\mathrm{ON,OFF}} e^{\lambda_{1,\mathrm{ON,OFF}}\theta} + B_{\mathrm{ON,OFF}} e^{\lambda_{2,\mathrm{ON,OFF}}\theta} \\ &\quad + \frac{V_S}{R_{\mathrm{ON,OFF}}} + K_{1,\mathrm{ON,OFF}} I_O \sin(\theta+\phi) \\ &\quad - K_{2,\mathrm{ON,OFF}} I_O \cos(\theta+\phi) \end{aligned} \tag{9}$$

where

$$\lambda_{1,\mathrm{ON,OFF}} = -\frac{1}{2\omega R_{\mathrm{ON,OFF}} C_P} + \frac{1}{\omega}\sqrt{\frac{1}{4R_{\mathrm{ON,OFF}}^2 C_P^2} - \frac{1}{C_P L_T}} \tag{10}$$

$$\lambda_{2,\mathrm{ON,OFF}} = -\frac{1}{2\omega R_{\mathrm{ON,OFF}} C_P} - \frac{1}{\omega}\sqrt{\frac{1}{4R_{\mathrm{ON,OFF}}^2 C_P^2} - \frac{1}{C_P L_T}} \tag{11}$$

$$\begin{aligned} K_{1,\mathrm{ON,OFF}} &= (1-\omega^2 C_P L_B)\frac{(1-\beta^2)R_{\mathrm{ON,OFF}}^2}{(1-\beta^2)^2 R_{\mathrm{ON,OFF}}^2 + \omega^2 L_T^2} \\ &\quad + \frac{\omega L_B}{R_{\mathrm{ON,OFF}}}\frac{\omega L_T R_{\mathrm{ON,OFF}}}{(1-\beta^2)^2 R_{\mathrm{ON,OFF}}^2 + \omega^2 L_T^2} \end{aligned} \tag{12}$$

$$\begin{aligned} K_{2,\mathrm{ON,OFF}} &= (1-\omega^2 C_P L_B)\frac{\omega L_T R_{\mathrm{ON,OFF}}}{(1-\beta^2)^2 R_{\mathrm{ON,OFF}}^2 + \omega^2 L_T^2} \\ &\quad - \frac{\omega L_B}{R_{\mathrm{ON,OFF}}}\frac{(1-\beta^2)R_{\mathrm{ON,OFF}}^2}{(1-\beta^2)^2 R_{\mathrm{ON,OFF}}^2 + \omega^2 L_T^2} \end{aligned} \tag{13}$$

$$\beta^2 = \omega^2 C_P L_T. \tag{14}$$

Note that A_{ON}, B_{ON}, A_{OFF}, and B_{OFF} in (9) are constants to be determined by the boundary conditions. Since I_C and V_P are periodic waveforms, they must satisfy the periodic condition. In addition, according to the electrical characteristics of inductance and capacitance, I_C and V_P must be continuous at the transition from switch-on to switch-off. These boundary conditions are written as

$$I_{C,\mathrm{ON}}(0) = I_{C,\mathrm{OFF}}(2\pi) \tag{15}$$

$$V_{P,\mathrm{ON}}(0) = V_{P,\mathrm{OFF}}(2\pi) \tag{16}$$

$$I_{C,\mathrm{ON}}(\pi) = I_{C,\mathrm{OFF}}(\pi) \tag{17}$$

$$V_{P,\mathrm{ON}}(\pi) = V_{P,\mathrm{OFF}}(\pi). \tag{18}$$

The classic Class-E condition sets the transistor output voltage and its differentiation both equal to zero at the transition from switch-off to switch-on ($\theta = 0$). This theory modifies this condition to allow a phase (or time) mismatch for the transistor output voltage set to zero at $\theta = \Delta\theta$, i.e.,

$$V_{P,\mathrm{ON}}(\Delta\theta) = 0, \qquad \text{for } \Delta\theta \geq 0$$

or

$$V_{P,\mathrm{OFF}}(\Delta\theta) = 0, \qquad \text{for } \Delta\theta < 0 \tag{19}$$

$$\left.\frac{dV_{P,\mathrm{ON}}(\theta)}{d\theta}\right|_{\theta=0} = 0. \tag{20}$$

Six variables, i.e., A_{ON}, B_{ON}, A_{OFF}, B_{OFF}, I_O, and ϕ can be solved from a set of linear equations by substituting (15)–(20) into (9). This determines the voltage and current waveforms at each node or branch of the circuit. The load network impedance can be further determined by performing the following integration:

$$Z_L = R_L + jX_L = \frac{j}{\pi I_O}\int_0^{2\pi} V_B(\theta) e^{-j(\theta+\phi)} d\theta. \tag{21}$$

As a result, the output power and consumed dc power can be calculated by

$$P_{\mathrm{out}} = \frac{I_O^2 R_L}{2} \tag{22}$$

$$P_{DC} = \frac{V_S}{2\pi}\int_0^{2\pi} I_C(\theta) d\theta. \tag{23}$$

where the ratio of (22)–(23) is defined as the dc-to-RF efficiency.

To validate the theory, the experiment uses a packaged GaAs pseudomorphic HEMT (pHMET) (FPD3000) to build a 1.95-GHz Class-E PA with a 3.3-V supply voltage. A first estimate of the transistor switch-on and switch-off resistances, output capacitance and drain bond-wire inductance came from the packaged transistor model [26] provided by the manufacturer, and was then confirmed by our conducted device model extraction to obtain the following element quantities at 1.95 GHz: $R_{\mathrm{ON}} = 0.8\ \Omega$, $R_{\mathrm{OFF}} = 650\ \Omega$, $C_P = 1.8$ pF, and $L_B = 0.6$ nH. After substituting these quantities into the derived analytical solution, Fig. 2(a) shows the predicted dc-to-RF efficiency and output power with respect to phase mismatch at various dc-feed inductances. Fig. 2(b) shows the calculated required load network impedance. It can be seen that the maximum dc-to-RF efficiency does not coincide with the classic Class-E condition to occur at 0° for $\Delta\theta$, but instead at several plus degrees. The output power corresponding to the maximum dc-to-RF efficiency increases with dc-feed inductance. Therefore, a larger dc-feed inductance is helpful to increase the output power. This experiment uses an 8.2-nH dc-feed inductor with a compromise of the inductor self-resonant frequency. For this dc-feed inductance value, the theory predicts a maximum dc-to-RF efficiency of 83% at $\Delta\theta = 8^\circ$ with a corresponding output power of 463 mW and a required load network impedance of $9.35 + j4.54\ \Omega$.

To consider the effects of tolerances due to variations in circuit parameters, Fig. 3 shows the simulated sensitivities to dc-to-RF efficiency and output power of the Class-E PA under the maximum dc-to-RF efficiency condition found above. It can be seen from Fig. 3 that the top three factors to sensitize the dc-to-RF efficiency are R_{ON}, R_L, and R_{OFF}, while in contrast, the top three factors to sensitize the output power are L_B, C_P, and X_L. Therefore, it is remarked that the switch-off resistance and bond-wire inductance, usually ignored by most of the reported Class-E PA design theory, are important to be included for accurate prediction of the dc-to-RF efficiency and output power at the same time.

From Fig. 2(a), one can also see that there exists a tradeoff between dc-to-RF efficiency and output power in a large range of $\Delta\theta$. The range begins at -74° for maximum output power and

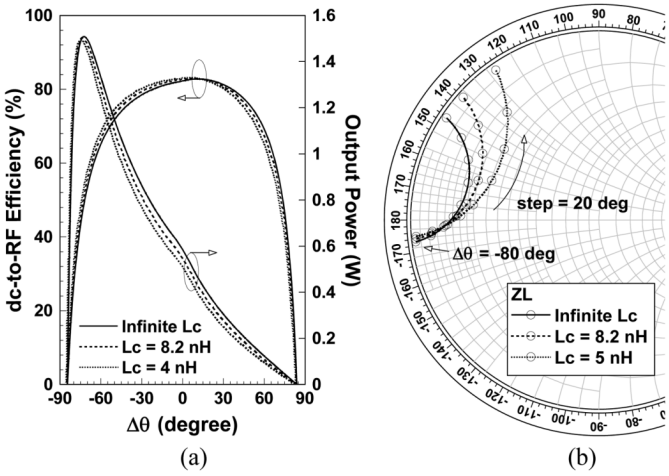

Fig. 2. RF parameters of Class-E PA considering phase mismatch and different dc-feed inductances at 1.95 GHz and 3.3-V supply voltage. (a) DC-to-RF efficiency and output power. (b) Load network impedance.

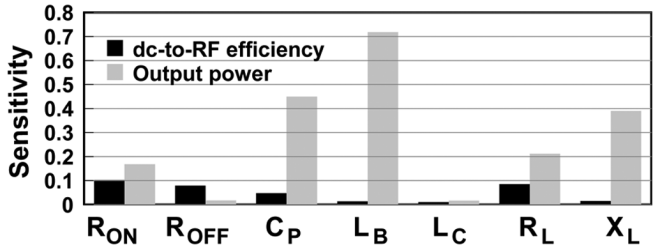

Fig. 3. Simulated sensitivities to dc-to-RF efficiency and output power of the Class-E PA with a phase mismatch of 8° and a dc-feed inductance of 8.2 nH.

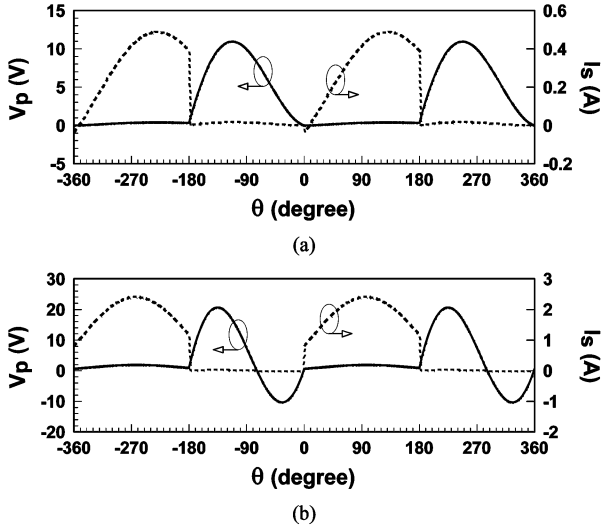

Fig. 4. Switching waveforms of the 1.95-GHz Class-E PA operating under modified Class-E conditions. (a) Maximum efficiency mode ($\Delta\theta = 8°$). (b) Maximum output power mode ($\Delta\theta = -74°$).

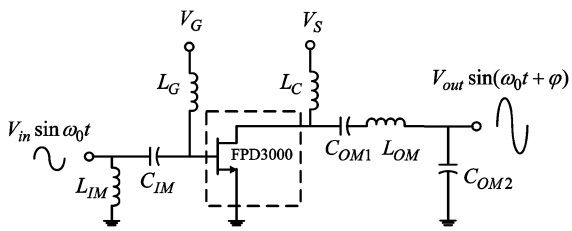

Fig. 5. Designed circuit schematic of the Class-E PA.

TABLE I
COMPARISON BETWEEN THEORETICAL AND MEASURED RESULTS FOR THE 1.95-GHZ CLASS-E PA DESIGN BASED ON MODIFIED CLASS-E CONDITION FOR MAXIMUM DC-TO-RF EFFICIENCY

Input parameters: V_S = 3.3 V, R_{ON} = 0.8 Ω, R_{OFF} = 650 Ω, C_P = 1.8 pF, L_B = 0.6 nH, L_C = 8.2 nH, $\Delta\theta$ = 8°		
Output parameters	Theory	Measurement
Consumed dc current	169 mA	167 mA
Output power	463 mW	450 mW
dc-to-RF efficiency	83 %	81.7 %

ends at 8° for maximum dc-to-RF efficiency. Fig. 4(a) and (b) shows the switching voltage and current waveforms at $\Delta\theta = 8°$ and $-74°$, respectively. It is noted that in Fig. 4(a) that the switching voltage and current waveforms have a very small overlap with each other, which gives the minimum switching loss ratio. In contrast, in Fig. 4(b), the switching voltage and current waveforms have a very large peak value, which leads to the maximum output power.

Fig. 5 shows the circuit schematic of the 1.95-GHz Class-E PA in the experiment. In Fig. 5, the output matching network matches the required load impedance $9.35 + j4.54\ \Omega$ to 50 Ω, and the input matching network performs a 50-Ω conjugate match for obtaining a higher gain and power-added efficiency (PAE). Table I compares the theoretical and measured results for the implemented Class-E PA. The comparison shows excellent agreement. From the measurements, this Class-E PA consumes a dc current of 167 mA from a 3.3-V supply, and delivers an output power of 450 mW (26.5 dBm) at an input power of 55 mW. The corresponding gain, PAE, and dc-to-RF efficiency is 9.1 dB, 71.7%, and 81.7%, respectively. Since the Class-E PA belongs to a switching-mode PA, it has the characteristic to increase output power as the square of the supply voltage with maintaining similar gain and efficiency.

Table II shows the comparison with other Class-E PA designs [25], [27], [28] including our previous works [20]–[24]. Note that this work differs from the previous ones by applying a modified Class-E condition to the Class-E PA design, and consequently achieves a dc-to-RF efficiency of 81.7%. This efficiency, to the best of the authors' knowledge, is the highest in the literature for Class-E PAs at above gigahertz frequencies.

III. LINEARIZATION APPROACH

A. Dynamic Supply Voltage Scaling

In the continuous-wave (CW) measurement of the Class-E PA, as illustrated in Fig. 5, Fig. 6(a) plots the measured gain and PAE with respect to the ratio of $V_{\rm in}$ to V_S by sweeping the input RF power under a fixed supply voltage of 4.2 V. One can see that the Class-E PA exhibits strong nonlinearity because of a large variation in gain response. The corresponding PAE has a maximum value of 72.3% at a $V_{\rm in}$-to-V_S ratio of 0.71. This ratio was used for setting the supply voltage proportional to the input RF amplitude to linearize the Class-E PA with maximum

TABLE II
PERFORMANCE COMPARISON AMONG VARIOUS CLASS-E PA DESIGNS

Reference	[28]	[25]	[27]	[20]-[22]	[23],[24]	This work
Frequency	5-6 GHz	900 MHz	950 MHz	1.95 GHz	1.95 GHz	1.95 GHz
Active device	SiGe HBT IC	SiGe HBT IC	Packaged MESFET	GaAs pHEMT IC	GaAs HBT IC	Packaged pHEMT
Load network	Lumped element	On chip	T-line element	Lumped element	Lumped element	Lumped element
Output power	20.1 dBm	20.2 dBm	26.6 dBm	26.5 dBm	24.5 dBm	26.5 dBm
dc-to-RF efficiency	58.4 %	71 %	72 %	56.4 %	57.3 %	81.7 %
Design condition	Class E	Class E	Class E	Class E	Class E	Modified Class E

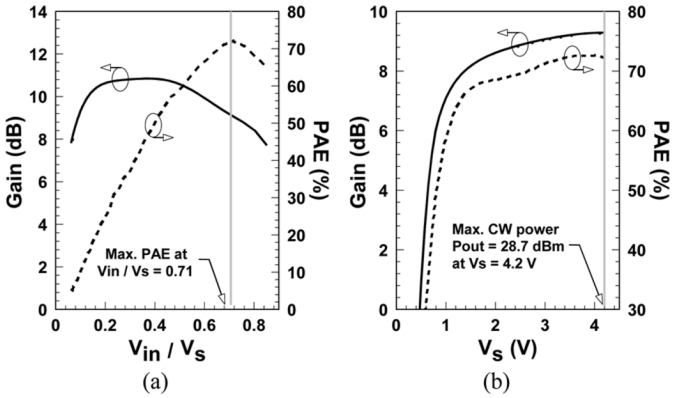

Fig. 6. CW measurements of the Class-E PA by sweeping input RF amplitude with fixed and dynamic supply voltages. (a) $Vs = 4.2$ V. (b) $Vs = Vin/0.71$.

PAE. As shown in the measurement results of Fig. 6(b), such a dynamic supply voltage scaling ($V_S = V_{\text{in}}/0.71$) results in an almost constant gain and PAE over a wide supply voltage range from 1.5 to 4.2 V. As the supply voltage equals 4.2 V, the gain and PAE reaches 9.2 dB and 72.3%, respectively, and the output power is 28.7 dBm, but as the supply voltage is below 1.5 V, both gain and PAE drop quickly. This is because the GaAs pHEMT cannot switch on and off properly when the applied input RF amplitude that is proportional to the supply voltage is at a low level.

In order to further improve the linearization results shown in Fig. 6(a), this paper employs digital predistortion to obtain a constant gain and phase delay (φ) over the entire supply voltage range from 0 to 4.2 V. Fig. 7(a) shows the AM/AM and AM/PM characteristic of Class-E PA by measuring the $V_{\text{out}} - V_S$ and $\varphi - V_S$ relation, respectively, with the help of a vector network analyzer. Fig. 7(a) also shows the linearization baselines for $V_{\text{out}} - V_S$ and $\varphi - V_S$ relations that have a base point at $V_S = 4.2$ V. A function, $g(V_S)$, is given for producing the predistorted supply voltage to make the corresponding output RF amplitude follow the $V_{\text{out}} - V_S$ linearization baseline. This can be mathematically described as

$$V_{\text{out}}\left(g\left(V_s\right)\right) = \frac{V_{\text{out}}(V_s = 4.2\text{V})}{4.2\text{V}} V_s = 2.05 \cdot V_s. \qquad (24)$$

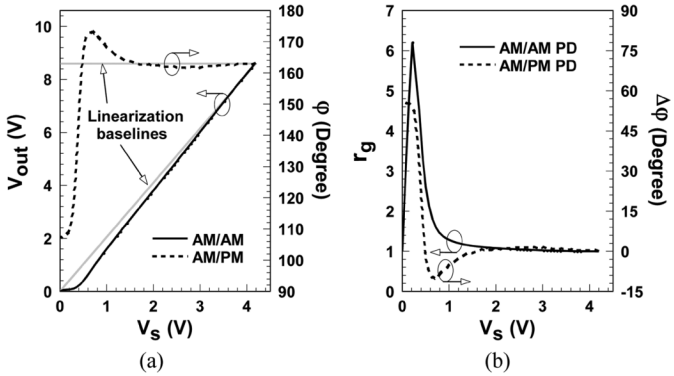

Fig. 7. Nonlinear relations and their predistortion functions for the Class-E PA using the dynamic supply voltage scaling technique. (a) AM/AM and AM/PM relations. (b) AM/AM and AM/PM predistortion functions.

An AM/AM predistortion function is then found as

$$r_g(V_s) = \frac{g(V_S)}{V_S} = \frac{V_{\text{out}}^{-1}(2.05 \cdot V_S)}{V_S} \qquad (25)$$

where represents the inverse function of the AM/AM relation shown in Fig. 7(a). To coincide with the $\varphi - V_S$ linearization baseline, the AM/PM relation shown in Fig. 7(a) needs to be compensated for the difference from the $\varphi - V_S$ linearization baseline. Therefore, the AM/PM predistortion function can be found as

$$\Delta\varphi(V_s) = \varphi(V_s = 4.2\text{V}) - \varphi(V_s) = 162.9^\circ - \varphi(V_s). \quad (26)$$

Fig. 7(b) shows both AM/AM and AM/PM predistortion functions according to the calculations in (25) and (26). Each predistortion function is uniformly sampled with the resolution of 64 samples over the supply voltage range from 0 to 4.2 V in building a lookup table (LUT) for use by the digital envelope predistorter (DEP) to be discussed subsequently.

B. DEP

Fig. 8 shows the proposed quadrature-modulation transmitter with an envelope-tracking PA for transmitting nonconstant envelope modulated signals. It consists of a DEP, a Class-S modulator, an IQ modulator, and a Class-E PA. The DEP takes charge of generating the predistorted baseband IQ and envelope signals for linearizing the Class-E PA. The Class-S and IQ modulator outputs the predistorted analog envelope signal and quadrature-modulated carrier signal to be inserted into the supply-voltage and RF-input terminal, respectively, of the Class-E PA.

Fig. 9 shows the block diagram of the DEP used in the transmitter architecture shown in Fig. 8. The input I and Q signals are serial bit streams of random data generated at a chip rate of 1.2288 Mc/s using the linear feedback shift registers. At first, the I and Q signals are pulse-shaped by the digital finite impulse response (FIR) filters at four times the chip rate and with the coefficients according to the cdma2000 1 $\times$ standard [29]. The half-band filters are then used to interpolate the pulse-shaped IQ signals with a sampling rate eight times the chip rate and also serve as a low-pass filter for suppressing the alias signal generated in the following up-sampling process. Output signals

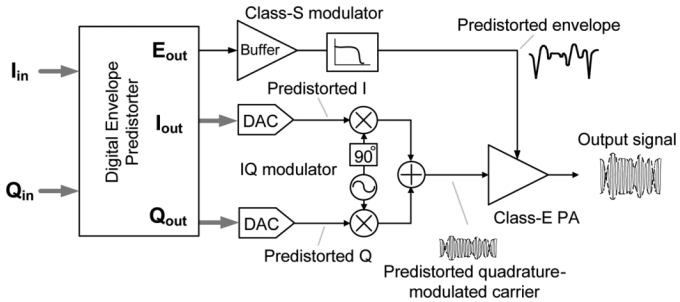

Fig. 8. Block diagram of the proposed quadrature-modulation transmitter using an envelope-tracking Class-E PA.

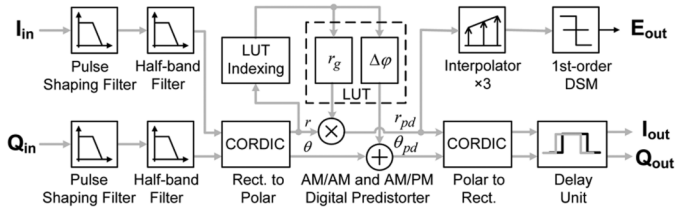

Fig. 9. Block diagram of the DEP.

from the half-band filter are fed to the coordinate rotation digital computer (CORDIC) unit for extraction of envelope and phase signals. The extracted envelope and phase signals are then input to a LUT-based AM/AM and AM/PM predistorter for compensating the AM/AM and AM/PM distortions of Class-E PA.

With the help of three linear interpolators, the predistorted envelope signal is further up-sampled to a sampling rate equal to 64 times the chip rate. This up-sampling process is necessary for the delta–sigma modulator to achieve a low quantization error. Power consumption becomes an important issue when the operating frequency is as high as 64 times the chip rate. A linear interpolator can be simply realized with an adder and a de-multiplexer and consumes much less dc power than a half-band filter. The delta–sigma modulator has a 1-bit first-order design, which can be realized using an accumulator. Its output binary signal is fed to a Class-S modulator that is composed of a buffer amplifier for amplification and a low-pass filter for analog waveform recovery of the predistorted envelope signal. The Class-S modulator efficiency evaluated as the ratio of the average envelope output power to the dc consumed power maintains about 80% in processing an envelope signal with bandwidth up to 5 MHz. This efficiency is an important factor in determining the dc-to-RF efficiency of the presented transmitter.

The predistorted envelope and phase signals enter another CORDIC for converting into the predistorted I and Q signals, then pass through the delay unit, and finally arrive at the digital-to-analog converters (DACs) for subsequent RF quadrature modulation. The use of predistorted I and Q signals together with the predistorted envelope signal aims to linearize the Class-E PA. The delay unit is constructed by a stack of registers, and compensates the time-delay difference between the envelope and quadrature-modulated signal paths.

The DEP is realized in a Xilinx Virtex-4 evaluation board. It delivers the predistorted envelope's DSM signal to be amplified and converted into an analog waveform fed to the supply-voltage terminal of Class-E PA. It also delivers the predistorted

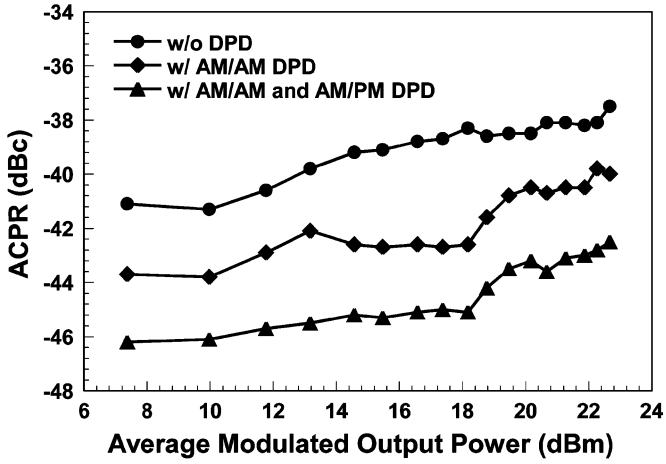

Fig. 10. Measured ACPRs for the implemented transmitter delivering cdma2000 1 × QPSK-modulated signals.

I and Q signals to be converted into analog signals and then digitally modulated onto the RF carrier as the input RF signal of Class-E PA.

IV. Experimental Results and Discussion

For demonstration, a prototype transmitter is implemented according to the architecture shown in Fig. 8 and used to generate cdma2000 1 × QPSK-modulated signals with 1.23-MHz modulation bandwidth. Considering that the PAPR is about 6 dB for this kind of transmit signal, the Class-E PA designed to have a maximum CW power of 28.7 dBm is available to deliver cdma2000 1 × signals with average modulated power up to 22.7 dBm.

The measured results for adjacent channel power ratio (ACPR) are demonstrated in Fig. 10. The results show that, depending on the digital predistortion scheme used, the ACPRs vary in a range of −46 to −38 dBc as the average modulated output power increases from 7 to 22.7 dBm. Compared to the results without using digital predistortion, the results with only AM/AM digital predistortion improve the ACPRs by 2–4 dB, while the results with both AM/AM and AM/PM digital predistortions improve the ACPRs by 5–7 dB. As an example, Fig. 11 shows the output spectra for comparing the predistortion effects on adjacent channel leakage power at the maximum output power of 22.7 dBm. It should be noted that the ACPR specification of cdma2000 1 × system is −42 dBc [30]. One can see from Fig. 10 that the simultaneous AM/AM and AM/PM digital predistortions assist the implemented transmitter to satisfy this ACPR specification over the entire available output power range.

Fig. 12 shows the measured error vector magnitudes (EVMs). It is observed that the EVMs without using digital predistortion vary from 4.7% to 5.2% over the entire available output power range. These EVMs are significantly improved by about 2.2% with the AM/AM digital predistortion, but only marginally further improved by about 0.2% with the additional AM/PM digital predistortion. Since the Class-E PA behaves quite linearly after using the proposed linearization approaches including dynamic supply voltage scaling and digital predistortion, the Class-S modulator and DACs used in the transmitter become the bottlenecks for ACPR and EVM performance. This

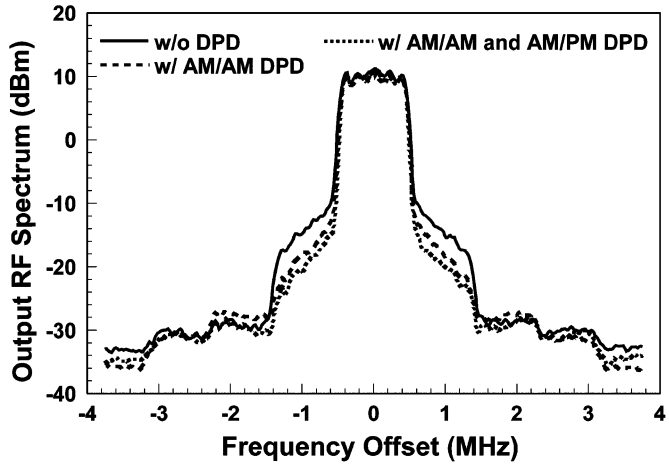

Fig. 11. Measured output RF spectra for the implemented transmitter delivering cdma2000 1 × QPSK-modulated signals at the maximum modulated output power of 22.7 dBm.

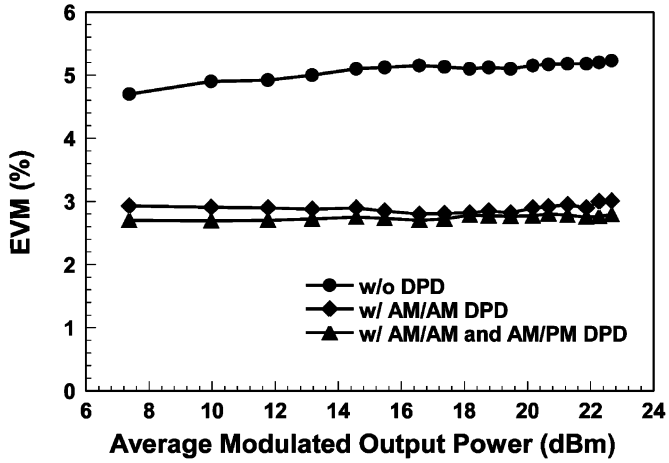

Fig. 12. Measured EVMs for the implemented transmitter delivering cdma2000 1 × QPSK-modulated signals.

can also account for the slight increase of ACPR and EVM with increasing output power because both the Class-S modulator and DAC components have a higher distortion as they process the signals with a larger envelope.

Defining the average dc-to-RF efficiency as the ratio of average modulated output power to consumed dc power for the Class-E PA along with Class-S modulator, we measured its dependence on average modulated output power, as shown in Fig. 13. This efficiency equals the product of the Class-E PA dc-to-RF efficiency and Class-S modulator efficiency for constant envelope modulated signals, but somewhat differently, this efficiency also depends on the signal distribution at various instantaneous envelope levels for nonconstant envelope modulated signals. After linearization, the Class-E PA provides a constant 9.2-dB power gain that is identical to the power gain at 4.2-V supply voltage. With knowledge of this power gain, the average PAE is calculated and also shown in Fig. 13. It is seen from Fig. 13 that the average dc-to-RF efficiency and PAE ranges from 49.6% to 61.3% and from 43.6% to 53.9%, respectively, in the entire available output power range. These results indicate that the presented transmitter has two important advantages compared to the linear PA-based ones. One is its

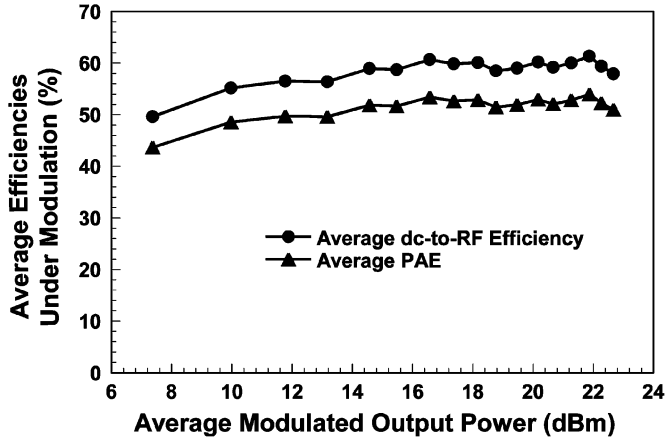

Fig. 13. Measured average efficiencies under modulation for the implemented transmitter delivering cdma2000 1 × QPSK-modulated signals.

remarkably high average efficiencies in delivering nonconstant envelope modulated signals. The other is that it drops in efficiency very slowly during power backoff. These advantages can dramatically enhance the average transmit efficiency of third-generation mobile communication systems that generally have high PAPR and transmit power control.

V. Conclusion

This paper has presented design and linearization methods for Class-E PAs applied to a quadrature modulation-based linear transmitter. At first, a high-efficiency Class-E PA design was carried out based on the proposed modified Class-E condition. The dynamic supply voltage scaling and digital predistortion techniques were then applied to linearize this Class-E PA by improving the PA AM/AM and AM/PM distortions. Consequently, the implemented quadrature modulation transmitter incorporating this Class-E PA has been identified as having high average efficiency properties in the application to a cdma2000 1 × system.

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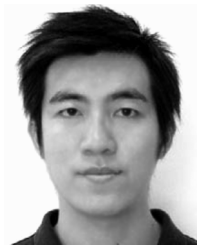

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