Envelope Following-Based RF Transmitters Using Switching-Mode Power Amplifiers

Je-Kuan Jau, *Student Member, IEEE*, Yu-An Chen, Tzyy-Sheng Horng, *Senior Member, IEEE*, and Jian-Yu Li

***Abstract*—This research presents a high-efficiency linear radio frequency transmitter applying the envelope-following technique to a switching-mode power amplifier. The use of predistorted envelope and quadrature-modulated signals can linearize the nonlinear behavior with fairly high average efficiency. The experimental results show that the proposed transmitter can deliver a 1.9-GHz CDMA2000 1× signal with high adjacent channel power ratio, low error vector magnitude, and high power added efficiency over a wide range of modulated output power.**

***Index Terms*—Envelope following, linear radio frequency (RF) transmitter, switching-mode power amplifier.**

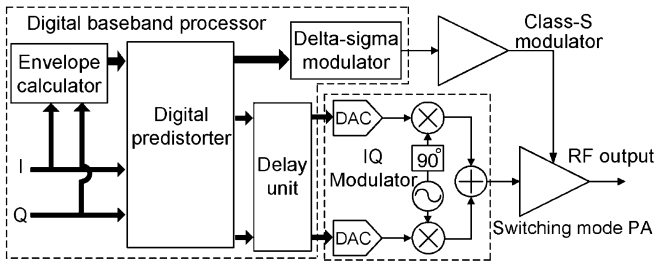

Fig. 1. Proposed envelope following-based RF transmitter using a switching-mode PA.

I. Introduction

MODERN digital communication systems usually apply the time-varying envelope modulation schemes, such as quadrature phase shift keying (QPSK) and quadrature amplitude modulation (QAM), to meet more stringent spectrum efficiency standards. The high peak-to-average power ratio (PAPR) in these modulation schemes usually requires a highly linear power amplifier (PA) with a sacrifice in efficiency. The envelope-following techniques in [1] and [2] can improve the linear PA's average efficiency by amplitude-modulating the supply voltage at the rate of the envelope variation via a Class-S modulator. This can let the supply voltage vary positively with the envelope level so as to save average dc power consumption.

The envelope-following technique proposed in this letter replaces the linear PA with a switching-mode PA to further enhance the efficiency. The switching-mode PA operates like a switch with a distinguishing feature that the voltage waveform across the transistor hardly overlaps the current waveform through the transistor. This way, the power dissipated at the transistor is relatively lower to achieve higher efficiency in comparison to the other high-efficiency PAs. In addition, a switching-mode PA, such as Class-E PA, has an inherently linear relation between supply voltage and RF-output amplitude and can be treated as an amplitude modulator for restoring the envelope through the supply voltage onto a phase-modulated carrier, as used in the envelope elimination and restoration (EER) transmitters [3], [4]. However, in the proposed technique, since both RF-input and supply-voltage signals applied to a switching-mode PA contain the envelope variation, the RF-output modulated signal should be distorted due to the double amplitude modulation. Therefore, this research aims to work out a feasible solution for the envelope following-based RF transmitters that can use very highly efficient switching-mode PAs. After careful study, a digital predistorter designed for AM–AM compensation is proposed to improve the output signal distortion. As a result, a prototype transmitter for 1.9-GHz CDMA2000 1× applications has been implemented and proved to be highly linear and efficient based on the proposed technique.

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II. System Overview and Implementation

The proposed transmitter system shown in Fig. 1 consists of a digital baseband processor, an IQ modulator, a Class-S modulator, and a switching-mode PA. The digital baseband processor mainly includes an envelope calculator, a predistorter, a delta–sigma modulator, and a delay unit. The envelope calculator aims to extract the envelope from the baseband pulse-shaped IQ signal in the digital domain. The predistorter is for compensating the above-mentioned AM–AM distortion due to the double amplitude modulation. The delta-sigma modulator is to replace the conventional pulse width modulator for driving the Class-S modulator. The delay unit is required to compensate the phase mismatch between phase information and amplitude information at the combination point. The Class-S and IQ modulator takes charge of delivering an amplified analog envelope signal and a quadrature-modulated RF signal to be inserted into the supply-voltage and RF-input terminal, respectively, of the switching-mode PA.

A. Class-E PA

The Class-E PA classified as a switching-mode PA is quite popularly used in the EER transmitters because of its high efficiency and good linear relation between supply voltage and RF-output amplitude. Fig. 2(a) illustrates a Class-E PA

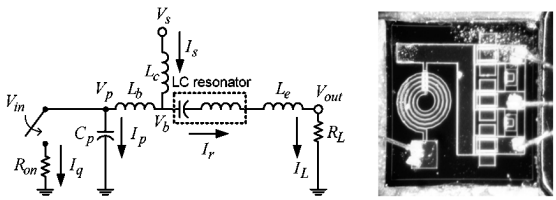

Fig. 2. (a) Equivalent circuit. (b) Chip micrograph of the designed Class-E PA.

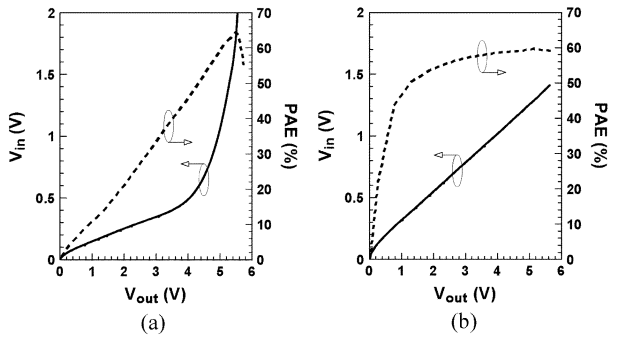

Fig. 3. RF input-output amplitude relation and PAE in the CW measurement of Class-E PA with (a) $V_s = 3$ V and (b) $V_s = 2.33V_{\rm in}$.

design for the specific application to our proposed RF transmitter. To ensure high efficiency, the on-chip output shunt capacitance (C_p) and off-chip output load-network elements in the Class-E PA must be carefully designed to eliminate as much waveform overlap as possible between the voltage (V_p) across and the current (I_q) through the power transistor. In addition, a small dc-feed inductance is used for increasing the modulation bandwidth at the supply-voltage terminal [5]. In [6], we have derived the closed-form design solutions for these output matching elements in simultaneous consideration of the switch-on resistance $(R_{\rm on})$, dc-feed inductance (L_c), and package bondwire inductance (L_b).

According to the derived solutions, the Class-E PA was implemented in a 0.15-μm InGaAs pHEMT process with a chip micrograph shown in Fig. 2(b), and then measured in continuous wave (CW) at a fixed and variable supply voltage (V_s) with results as shown in Fig. 3(a) and (b), respectively. It can be seen from Fig. 3(a) that at a fixed V_s of 3 V, the Class-E PA exhibits strong nonlinearity in the RF input-output amplitude relation with a power added efficiency (PAE) decreasing almost linearly from the peak value of 64% to a lower value as the RF-output amplitude is decreased. To linearize the Class-E PA, a variable supply voltage in proportion to the RF-input amplitude $(V_{\rm in})$ is applied. In Fig. 3(a), at $V_s = 3$ V, the voltage gain is equal to 12 dB $(G_v = 3.98)$ for $V_{\rm in} = 1.29$ V ($V_{\rm out} = 5.13$ V). Hence, the value of $V_s/V_{\rm in}$ is 2.33, which is chosen as the constant ratio to achieve the targeted 12-dB constant gain for all input amplitude levels up to 1.29 V. From the measurement results shown in Fig. 3(b), such an amplitude-following supply voltage not only improves the linearity but also enhances the PAE quite noticeably for all output amplitude levels up to 5.13 V.

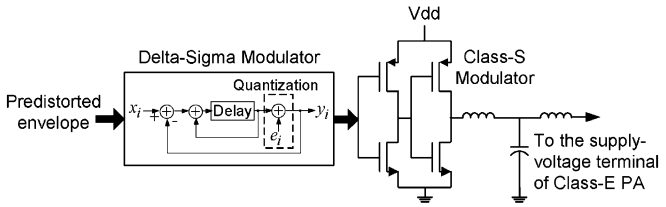

Fig. 4. Class-S modulator driven with the delta–sigma modulator for high-efficiency envelope processing.

B. Digital Predistortion Scheme

When the RF-input amplitude is large enough to switch the power transistor between saturation and cut-off, the Class-E PA can achieve a linear relation between RF-output amplitude and supply voltage with a high PAE up to 60%, as shown in Fig. 3(b). However, at low RF-input amplitudes, the power transistor cannot switch on and off properly. Due to that, the Class-E PA reduces the gain and thus cannot maintain the linear $V_{\rm in}$–$V_{\rm out}$ relation anymore. In this research, a digital predistortion scheme is proposed to overcome this problem. The measured $V_{\rm in} - V_{\rm out}$ relation shown in Fig. 3(b) can be expressed as

$$V_{\rm in}(V_{\rm out}) = \frac{V_{\rm out}}{G_v} + \Delta V(V_{\rm out}) \tag{1}$$

where ΔV is the voltage error to account for the deviation from the linear part that corresponds to the targeted 12-dB constant gain. From (1), ΔV can be compensated for by designing a digital predistorter to modify $V_{\rm in}$ as

$$V_{\rm in}^{'} = V_{\rm in} + \Delta V(G_v V_{\rm in}). \tag{2}$$

It is noted that ΔV is a smoothly varying function and can be curve-fitted as a polynomial for the purpose of implementing the predistorter as a digital arithmetic unit. In a digital modulation test, $V_{\rm in}$ can be regarded as equal to the transient envelope of the applied quadrature-modulated signal.

C. Envelope Processing Technique

As shown in Fig. 4, a class-S modulator driven with a first-order delta–sigma modulator is used for processing the envelope signal highly efficiently. The delta–sigma modulator aims to transform an input multibit envelope signal into a binary one and its operation can be described in the z-transform domain as

$$y = xz^{-1} + e(1 - z^{-1}) \tag{3}$$

where x and y are the input multi-bit signal and the output 1-b binary signal, respectively, and e represents the quantization error. From (3), the output signal is regarded as unchanged except for a unit delay while the quantization error is differentiated. Due to the differentiation, the resulting quantization noise is pushed to high frequency. The Class-S modulator consists of a CMOS buffer realized in a 0.35-μm CMOS process to amplify the binary envelope signal, and a third-order equal-ripple Chebyshev low-pass filter as an output stage to further convert the binary envelope signal into an analog one with the filtered

out quantization noise. The envelope processing efficiency is defined as the ratio of the average envelope output power to the dc consumed power, which is given as

$$\eta_e = \frac{P_{\rm env}}{P_{\rm dc}}. \tag{4}$$

In the measurement, η_e varies within 70%–80% in the applicable range of average envelope output power.

D. Baseband Processor and IQ Modulator

The baseband processor finally implemented using FPGA includes the pulse-shaping filter, half-band filter, interpolator, envelope calculator, predistorter, delay unit, and delta–sigma modulator. The pulse-shaping filter operates at four times the chip rate of 1.2288 Mcps by following the CDMA2000 1× standard. Then, the half-band filter is used to interpolate the pulse-shaped IQ signals with a sampling rate eight times the chip rate before inserting them into the envelope calculator and subsequently into the predistorter, delay unit, and IQ modulator. Before entering the delta–sigma modulator, the first component on the envelope-following path, a linear interpolator is used to further increase the sampling rate up to 32 times the chip rate. In implementation, the envelope calculator is realized based on the coordinate rotation digital computer (CORDIC) algorithm [7] for extracting the envelope from the pulse-shaped IQ signals. The predistorter is a digital arithmetic unit synthesized according to the curve-fitted polynomial for compensating the distortion resulting from the nonlinear $V_{\rm in}$–$V_{\rm out}$ relation. The delay unit constructed by a stack of registers is to compensate the time delay difference between the envelope-following and quadrature-modulated signal paths. It is noted that the delay unit has been tuned to have the optimum modulation quality. The IQ modulator mainly relies on a vector signal generator equipped with a two-channel digital-to-analog converter (DAC). It can output a 1.9-GHz QPSK-modulated CDMA2000 1× signal with error vector magnitude (EVM) typically less than 1%.

III. Experimental Results

The implemented prototype transmitter is applied to generate the QPSK-modulated CDMA2000 1× signal at the frequency of 1.9 GHz. Considering that the PAPR is about 6 dB for the QPSK modulation, the Class-E PA having a peak CW output power of 27 dBm is qualified to output the standard CDMA2000 1× signal with an average power up to about 21 dBm. The PAE for the prototype transmitter can be evaluated as

$$\begin{aligned}{\rm PAE} &= \frac{P_{\rm out} - P_{\rm in}}{P_{\rm dc}} \\ &= \frac{P_{\rm out} - P_{\rm in}}{P_{\rm env}} \cdot \frac{P_{\rm env}}{P_{\rm dc}} = {\rm PAE}' \cdot \eta_e \end{aligned} \tag{5}$$

where $P_{\rm out}$ and $P_{\rm in}$ represent the average modulated power at the output and input, respectively. In (5), the PAE can be also expressed as the product of the PAE with respect to Class-E PA (denoted by PAE′) and the envelope processing efficiency. It is particularly noted that the PAEs evaluated for the Class-E PA in the digital modulation test are approximately 10%–20% smaller, depending on the average modulated output power, than those in the CW test.

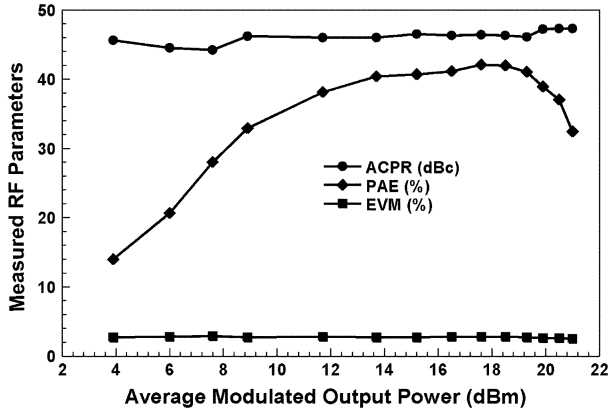

Fig. 5. Measured RF parameters for the proposed EER transmitter applied to the generation of a 1.9-GHz CDMA2000 1× signal.

Fig. 5 shows the measured PAE, EVM, and ACPR for the prototype transmitter. It can be seen that the prototype transmitter can achieve an almost constant EVM and ACPR value of about 2.7% and 47 dBc, respectively, over more than a decade range of average modulated output power from 4 to 21 dBm. The PAE exceeds 30% as the average modulated power is above 8 dBm, but drops quickly below that power level. This can be explained by Fig. 3(b), which displays a high descending rate for $V_{\rm out}$ smaller than 0.8 V (about 8 dBm in CW power). Nevertheless, the prototype transmitter still has much better overall efficiency than the conventional transmitter using a linear PA when applied to today's 3G CDMA systems with transmit power control.

IV. Conclusion

A promising envelope following-based RF transmitter that uses a switching-mode PA has been presented to achieve high ACPR, low EVM, and high PAE for application to a wideband and high PAPR wireless system. The success of having such a high performance is attributed to the fact that the applied predistorted envelope and quadrature-modulated signals can effectively linearize the switching-mode PA with high average efficiency.

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