

High-Performance Frequency-Hopping Transmitters Using Two-Point Delta-Sigma Modulation

Kang-Chun Peng, *Student Member, IEEE*, Chien-Hsiang Huang, Chien-Jung Li, and Tzyy-Sheng Horng, *Member, IEEE*

Abstract—This paper presents a 2.4-GHz high-performance frequency-hopping (FH) transmitter using two-point delta-sigma modulation (TPDSM). Two bottleneck problems in the implementation have been studied rigorously. One is the nonlinear performance of a phase-locked loop (PLL). The other is the inherent gain and delay mismatches between two modulation points. Both nonlinear and mismatch factors dominate the modulation accuracy in the closed PLL. Our formulation can predict the dependencies of modulation accuracy on both factors quite successfully. Comparison of the averaged frequency deviation and frequency-shift-keying (FSK) error between theory and measurement shows excellent agreement. The implemented TPDSM-based FH Gaussian FSK transmitter can achieve 2.5-Mb/s data rate along with 15- μ s PLL stable time with only 2.2% FSK error under good design and operating conditions.

Index Terms—Fractional- N synthesizer, frequency hopping (FH), phase-locked loop (PLL), two-point delta-sigma modulation (TPDSM).

I. INTRODUCTION

FOR frequency-hopping spread-spectrum (FHSS) transmitters, low power, high integration, fast hopping rate, as well as high system throughput are the main design considerations. Recently, the transmitter adopting the two-point delta-sigma modulation (TPDSM) architecture proposed in [1] has been applied to FHSS systems such as Bluetooth [2], [3]. In a TPDSM architecture, as shown in Fig. 1, there are two modulation points for the voltage-controlled oscillator (VCO). One point, which is from the fractional- N synthesizer, mainly provides the accurate carrier frequency. The other point, from the baseband transmit signal passing through a digital-to-analog converter (DAC) and filter, mainly performs the frequency modulation. The output frequency-modulated signal is then fed back to the divider in a phase-locked loop (PLL). Inside the divider, the data information from feedback path cancels out that from delta-sigma modulator (DSM) in the synchronous condition. This explains why the modulation bandwidth of TPDSM is not restricted in a closed PLL structure. Therefore, TPDSM not only maintains high data-rate modulation within a closed PLL, but also excludes the use of RF mixers. RF circuitry of TPDSM can be implemented with low cost and high integration, as well as the one of conventional open-loop architecture [4], but without the

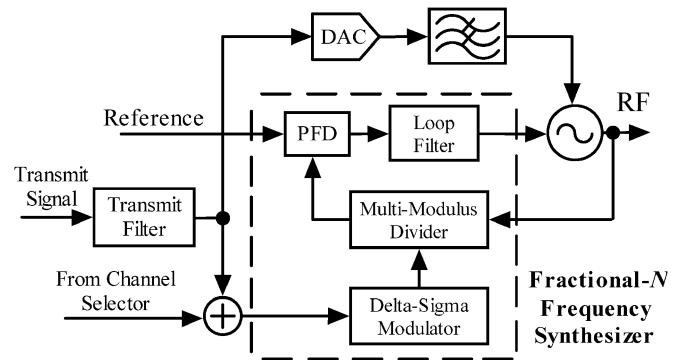


Fig. 1. TPDSM architecture for an FH RF transmitter.

problem of carrier frequency drift. In comparison with another quadrature modulation architecture, TPDSM can achieve the same high data rate with relatively lower power consumption [5].

The fractional- N frequency synthesizer, i.e., the core of TPDSM, can also provide very fast channel switching speed. In addition, TPDSM can be further combined with the polar modulation technique, which generates time-varying envelope modulation signals with significant efficiency [6]. These useful features also make TPDSM quite attractive in direct-sequence spread-spectrum (DSSS) applications.

TPDSM has its inherent drawbacks. The nonlinearity in PLL components and the mismatches between two modulation points often cause significant modulation distortion. These effects are hard to understand and, therefore, the need for good prediction methods is highly demanded in practical designs. With the help of a profound study on the mechanisms of PLL nonlinearity and frequency modulation, we successfully derive the compact formula for predicting the modulation accuracy in the TPDSM-based RF transmitters.

II. SYSTEM ANALYSIS

A. Nonlinear Characteristics in PLL Components

In principle, a well-designed fractional- N synthesizer can effectively suppress the phase noises from several major sources including the VCO, reference, and DSM by itself. However, this advantageous effect is counteracted when nonlinearity exists in a PLL [7]. This is because nonlinearity causes the phase intermodulation products that finally contribute to the phase noises. The PLL nonlinearity mainly results from the detection dead zone in a phase frequency detector (PFD) and the mismatch between the source and sink currents in a charge pump. Fig. 2

Manuscript received April 21, 2004; revised July 10, 2004. This work was supported by the National Science Council, Taiwan, R.O.C., under Grant NSC92-2213-E-110-012.

The authors are with the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung 804, Taiwan, R.O.C. (e-mail: d8931814@student.nsysu.edu.tw).

Digital Object Identifier 10.1109/TMTT.2004.837156

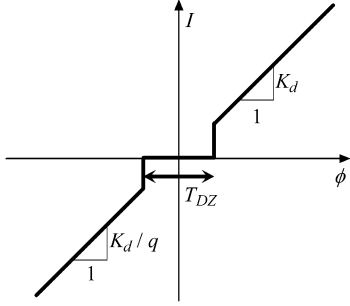


Fig. 2. Nonlinear input-output relation for the combined model of the PFD and charge pump.

shows a combined model of the PFD and charge pump with a nonlinear relation between the input PFD phase error and the output charge-pump current. The parameter T_{DZ} denotes the PFD dead-zone duration, and K_d denotes the combined gain of the PFD and charge pump in the charging process. When the charge pump is operated in the discharging process, a mismatch factor q must be considered, as well as that the combined gain is equal to K_d/q . In a previous study, we analyzed that the DSM quantization noise ($\phi_{n,DSM}$) is dominant over the other possible sources in a fractional- N synthesizer to cause the phase intermodulation products [8]. Therefore, we can focus on formulating the charge-pump output current noise due to $\phi_{n,DSM}$ in the time domain, which is given as

$$\begin{aligned} I_{n,DSM} &= K_d \cdot (\phi_{n,DSM} + \phi_{n,PFD} + \phi_{n,CP}) \\ &= K_d \phi'_{n,DSM} \\ &= K_d \phi_{n,DSM} + I_{n,PFD} + I_{n,CP} \end{aligned} \quad (1)$$

where

$$\phi_{n,PFD} = \begin{cases} -\phi_{n,DSM}, & |\phi_{n,DSM}| \leq T_{DZ} F_{ref} \pi \\ 0, & |\phi_{n,DSM}| > T_{DZ} F_{ref} \pi \end{cases} \quad (2)$$

$$\phi_{n,CP} = \begin{cases} (q-1)\phi_{n,DSM}, & \phi_{n,DSM} \geq 0 \\ 0, & \phi_{n,DSM} < 0 \end{cases} \quad (3)$$

$$I_{n,PFD} = K_d \phi_{n,PFD} \quad (4)$$

$$I_{n,CP} = K_d \phi_{n,CP}. \quad (5)$$

It is noted that F_{ref} denotes the reference frequency. From (1), $\phi_{n,PFD}$ and $\phi_{n,CP}$ can be regarded as the phase intermodulation noise due to the nonlinearity of the PFD and charge pump, respectively. $I_{n,PFD}$ and $I_{n,CP}$ in (4) and (5) are the corresponding current noises at the output of the charge pump. It is also noted that $\phi'_{n,DSM}$ is the equivalent DSM quantization noise after including both nonlinear intermodulation noises.

In our practical design for a fractional- N synthesizer, the PLL uses a differential active loop filter behind the PFD to avoid the use of a charge pump. This makes the PFD with a dead-zone duration of approximately 400 ps become the dominant nonlinear component. The reference frequency is chosen at 20 MHz. The DSM design adopts the well-known multistage noise-shaping (MASH) schemes. For comparison, two different schemes, i.e., MASH 1-1 and MASH 1-1-1, equivalent to the second- and third-order DSM, respectively, are used in our design. Their corresponding $\phi_{n,DSM}$ can be obtained from the residual phase errors in the quantization of divider modulus. By assuming a

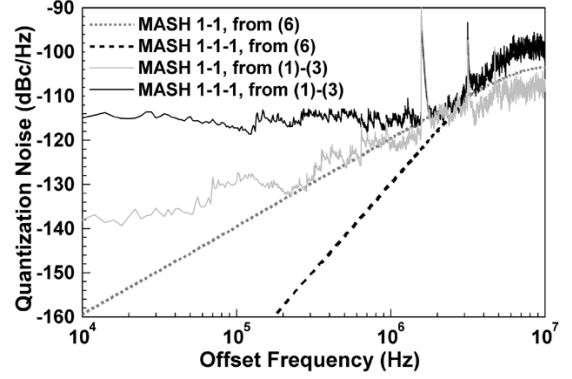


Fig. 3. Frequency-domain simulation of the DSM quantization noises in consideration of PLL nonlinearity in the fractional- N synthesizer design.

Gaussian distribution for such phase errors due to quantization [9], the frequency-domain expression of $\phi_{n,DSM}$ can be derived as

$$\phi_{n,DSM}(f) = \frac{\pi}{N\sqrt{3}} \left[2 \sin \left(\frac{\pi f}{F_{ref}} \right) \right]^{(m-1)}. \quad (6)$$

Equation (6) reveals that the higher DSM order (m) can push more quantization noises within $F_{ref}/2\pi$ to higher offset frequencies.

According to the nonlinear model depicted in Fig. 2, the equivalent DSM quantization noise ($\phi'_{n,DSM}$) in consideration of the nonlinear intermodulation noises can be evaluated using (1)–(3), and their simulated results are shown in Fig. 3. Generally speaking, the nonlinear intermodulation causes the spectral regrowth for the noise spectrum, which is especially obvious at lower offset frequencies, as can be seen in Fig. 3. This degenerates the DSM's ability of pushing quantization noise from a lower offset frequency to a higher offset frequency. Besides, the DSM cannot eliminate some fractional spurs present in the high offset frequency range effectively. Therefore, the PLL needs to increase its design complexity for suppressing these high-frequency fractional spurs. Fig. 3 also shows that the MASH 1-1-1 design has an average of 10-dB higher quantization noise than the MASH 1-1 design at lower offset frequencies. This is because the higher order MASH always causes larger variation of ϕ_{PFD} in the time domain and, consequently, arouses more nonlinear intermodulation noises in the frequency domain. It is also revealed from (2) and (3) that a PLL with a larger PFD dead-zone duration or charge-pump mismatch factor will deteriorate such a spectral regrowth more rapidly.

B. Mismatch Between Two Modulation Points

The model for TPDSM architecture shown in Fig. 1 is proposed as shown in Fig. 4 for analyzing the influence of mismatches between two modulation points. It is noted that τ and G_m represent the delay difference and gain deviation, respectively, between two modulation points. The PLL parameters include the combined gain of the PFD and charge pump in the charging process (K_d), and the tuning sensitivity of the VCO (K_v). The transfer function $F(S)$ represents the frequency response of the loop filter. The divider modulus is

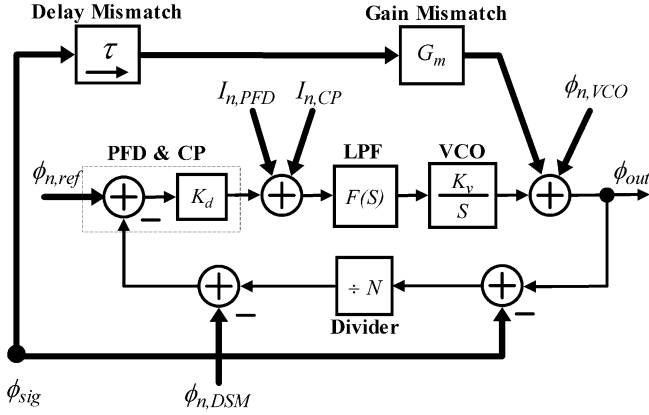


Fig. 4. Model for TPDSM-based RF transmitter.

equal to N . The noise parameters include $I_{n,PFD}$ and $I_{n,CP}$, whose time-domain expressions have been given in (4) and (5) for representation of the equivalent current noise due to the nonlinearity of the PFD and charge pump, respectively. The phase noises from the VCO, reference, and DSM are denoted by $\phi_{n,VCO}$, $\phi_{n,ref}$, and $\phi_{n,DSM}$, respectively. The transmit phase signal is represented by ϕ_{sig} . From the model, we can formulate the output phase signal as

$$\phi_{out} = \phi_{sig} H_a(S) + \phi_n \quad (7)$$

where

$$H_a(S) = \frac{H(S)}{N} + e^{-S\tau} G_m H_e(S) \quad (8)$$

$$\phi_n = (\phi_{n,ref} + \phi'_{n,DSM}) H(S) + \phi_{n,VCO} H_e(S) \quad (9)$$

$$H(S) = \frac{N K_v K_d F(S)}{N S + K_v K_d F(S)} \quad (10)$$

$$H_e(S) = \frac{N S}{N S + K_v K_d F(S)}. \quad (11)$$

Recall from (1) that $\phi'_{n,DSM} = \phi_{n,DSM} + \phi_{n,PFD} + \phi_{n,CP}$, and $\phi'_{n,DSM}$ is the equivalent DSM quantization noise in consideration of the PLL nonlinearity. Equation (7) shows that the output phase signal is equal to the multiplication of the transmit phase signal and the system transfer function $H_a(S)$ plus a phase noise term ϕ_n . From (8), we know that $H_a(S)$ mainly accounts for the two-point mismatch effects. This is because $H_a(S)$ equals unity when both mismatch factors disappear, i.e., $\tau = 0$ and $G_m = 1$. Under such circumstances, the input signal can be modulated without distortion and bandwidth limitation, but accompanies a residual phase noise equal to ϕ_n . Therefore, we can find ϕ_n practically by measuring the phase noise of output carrier from the fractional- N synthesizer without applying any modulated signal ($\phi_{sig} = 0$). For an adequate PLL design, the related transfer functions, i.e., $H(S)$ and $H_e(S)$, act as a low- and high-pass filter, respectively, to filter out most of the noise components according to (9). Therefore, under the two-point mismatch condition, $H_a(S)$ in (8) can be regarded as the dominant factor to determine the modulation accuracy.

For evaluating the two-point mismatch effects on Gaussian frequency-shift-keying (GFSK) modulation, the instantaneous Gaussian baseband signal is expanded in Fourier series as

$$d(t) = \sum_m A_m e^{j2\pi f_m t}. \quad (12)$$

The instantaneous frequency variation can then be written as

$$f_{sig}(t) = K_f d(t) = \sum_m K_f A_m e^{j2\pi f_m t} = \sum_m \Delta f e^{j2\pi f_m t} \quad (13)$$

where K_f and Δf represent the frequency-modulation sensitivity and GFSK frequency deviation, respectively. Integration of (13) yields the instantaneous phase signal. After taking the Fourier transform, the frequency response of transmit phase signal $\phi_{sig}(f)$ is derived as

$$\begin{aligned} \phi_{sig}(f) &= \Im\{\phi_{sig}(t)\} \\ &= \Im\left\{2\pi \int_0^t f_{sig}(t) dt\right\} \\ &= \sum_m \Delta f \frac{\delta(f - f_m)}{j f_m}. \end{aligned} \quad (14)$$

Assuming that the phase noise term ϕ_n in (7) is negligible under the two-point mismatch condition, the frequency response of the output phase signal can be approximated as

$$\begin{aligned} \phi_{out}(f) &\approx \phi_{sig}(f) H_a(S = j2\pi f) \\ &= \sum_m \Delta f_{sig}(f) \frac{\delta(f - f_m)}{j f_m} \end{aligned} \quad (15)$$

where

$$\Delta f_{sig}(f) = \Delta f H_a(S = j2\pi f). \quad (16)$$

From (16), it is known that $H_a(S)$ causes the frequency dependence of frequency deviation for the output GFSK signal. Fig. 5 shows the simulated magnitudes of $H_a(S)$ against offset frequency normalized by the PLL bandwidth (f_n) in consideration of certain mismatches between the two modulation points. It is found that the delay difference and gain deviation are both responsible for causing the frequency-dependent variations in the magnitude of $H_a(S)$. These variations are especially evident at the offset frequencies close to the PLL bandwidth.

The averaged frequency deviation (Δf_{avg}) and frequency-shift-keying (FSK) error are the most common parameters for determining the modulation accuracy of GFSK signal. Their values can be found from the following definitions [10]:

$$\Delta f_{avg} = E[\Delta f H_a(f)], \quad \text{for } |f| \leq \frac{B_{RF}}{2} \quad (17)$$

$$\begin{aligned} \text{FSK error} &= \frac{\text{rms}[\Delta f_{sig}(f) - \Delta f_{avg}]}{\Delta f_{avg}} \times 100\% \\ &= \frac{\Delta f_{sig-std}}{\Delta f_{avg}} \times 100\%, \quad \text{for } |f| \leq \frac{B_{RF}}{2} \end{aligned} \quad (18)$$

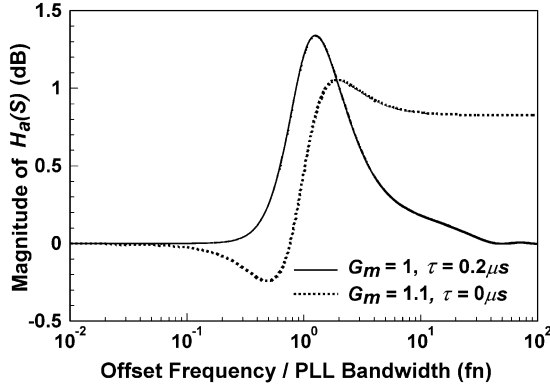


Fig. 5. Simulated magnitudes of $H_a(S)$ versus normalized offset frequency under the mismatch conditions of $G_m = 1$, $\tau = 0.2 \mu s$ and $G_m = 1.1$, $\tau = 0 \mu s$.

where B_{RF} denotes the RF channel bandwidth, and $\Delta f_{sig-std}$ denotes the standard deviation of $\Delta f_{sig}(f)$ within B_{RF} . In consideration with the residual phase noise ϕ_n , (17) can be rewritten as

$$\begin{aligned}\Delta f_{avg} &= E[\Delta f H_a(f) + \Delta f_n] \\ &= E[\Delta f H_a(f)] + E[\Delta f_n] \\ &= E[\Delta f H_a(f)], \quad |f| \leq \frac{B_{RF}}{2}\end{aligned}\quad (19)$$

where Δf_n denotes the frequency deviation caused by ϕ_n , and is treated as an independent random variable with a zero mean value. Meanwhile, (18) should be also reformulated as

$$\begin{aligned}\text{FSK error} &= \frac{\text{rms}[\Delta f_n(f) + \Delta f_{sig}(f) - \Delta f_{avg}]}{\Delta f_{avg}} \times 100\% \\ &= \frac{\sqrt{\Delta f_{n-rms}^2 + \Delta f_{sig-std}^2}}{\Delta f_{avg}} \times 100\%, \\ &\text{for } |f| \leq \frac{B_{RF}}{2}\end{aligned}\quad (20)$$

where Δf_{n-rms} represents the root-mean-square value of Δf_n , and can be theoretically expressed as a function of ϕ_n in the following form [11]:

$$\Delta f_{n-rms} = \sqrt{2 \times \int_0^{B_{RF}/2} \frac{\phi_n^2(f)}{B_{RF}} f^2 df}. \quad (21)$$

Under the two-point match condition, $\Delta f_{sig-std}$ vanishes such that Δf_{n-rms} can be measured from direct detection of the FSK error for the output GFSK signal. An alternative way for evaluating Δf_{n-rms} is to find ϕ_n by measuring the phase noise of the output carrier from the fractional- N synthesizer, and then substitute it into (21) for calculation of Δf_{n-rms} .

III. SIMULATED AND EXPERIMENTAL RESULTS

A 2.4-GHz frequency-hopping (FH) transmitter based on the TPDSM architecture has been implemented to transmit a GFSK signal with a data rate up to 2.5 Mb/s. The transmitter consists of two major parts, which are the: 1) mixed signal circuitry and

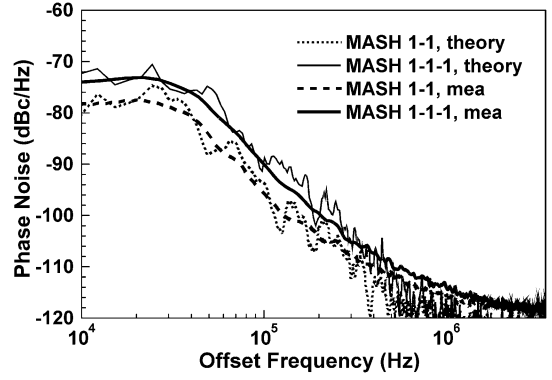


Fig. 6. Simulated and measured phase noises for the output carriers of the MASH 1-1 and MASH 1-1-1 fractional- N synthesizers with the PLL bandwidth set at 25 kHz.

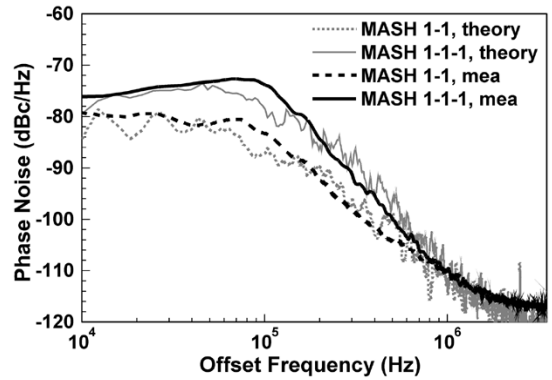


Fig. 7. Simulated and measured phase noises for the output carriers of the MASH 1-1 and MASH 1-1-1 fractional- N synthesizers with the PLL bandwidth set at 100 kHz.

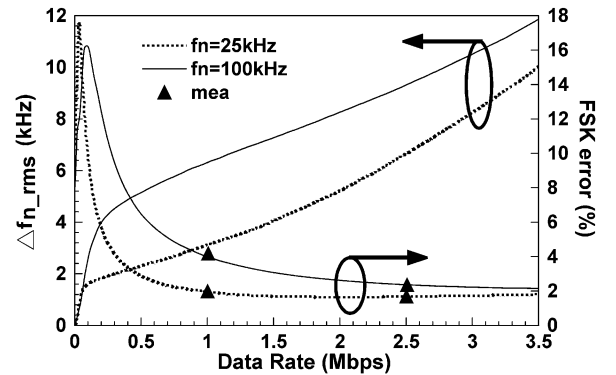


Fig. 8. Evaluation of Δf_{n-rms} and FSK errors under different data rates using the measured phase noises of output carriers from the MASH 1-1 fractional- N synthesizer.

2) baseband processor. The mixed signal circuitry includes the 2.4-GHz VCO with two tuning inputs, PLL components, and DAC. The baseband processor, including the DSM and digital Gaussian filter, is realized using a field-programmable gate array (FPGA). Most of the PLL parameters have been mentioned in the previous simulation of its nonlinear intermodulation. In the following experiments, the PLL bandwidth is particularly chosen at 25 and 100 kHz for comparing the performance difference. The bandwidth-time (BT) product of the Gaussian filter and modulation index are set at 0.5 and 0.315, respectively.

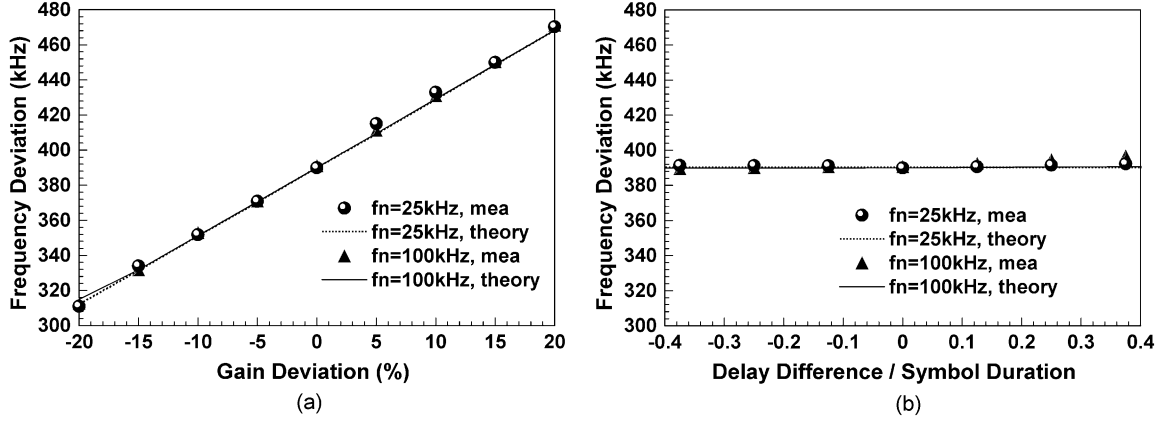


Fig. 9. Calculated and measured averaged frequency deviations versus: (a) gain deviation and (b) normalized delay difference for the TPDSM-based GFSK transmitters adopting the MASH 1-1 design with different PLL bandwidths.

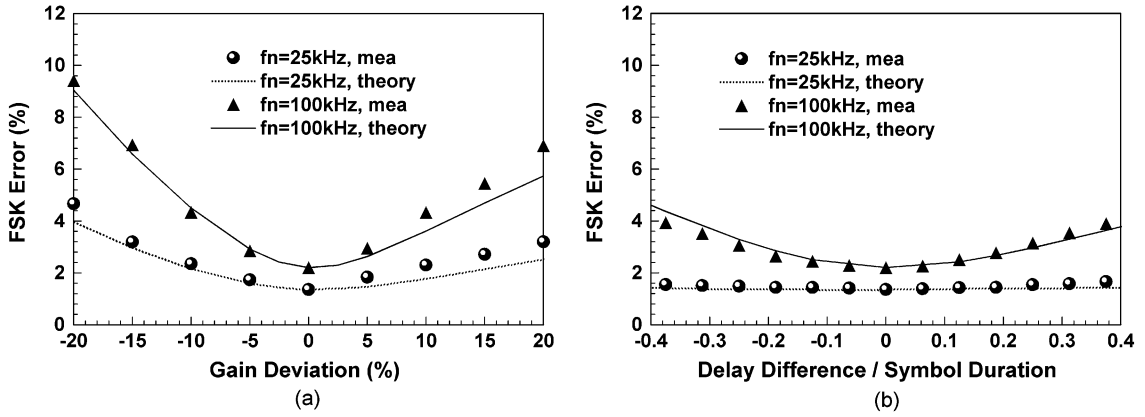


Fig. 10. Calculated and measured FSK errors versus: (a) gain deviation and (b) normalized delay difference for the TPDSM-based GFSK transmitters adopting the MASH 1-1 design with different PLL bandwidths.

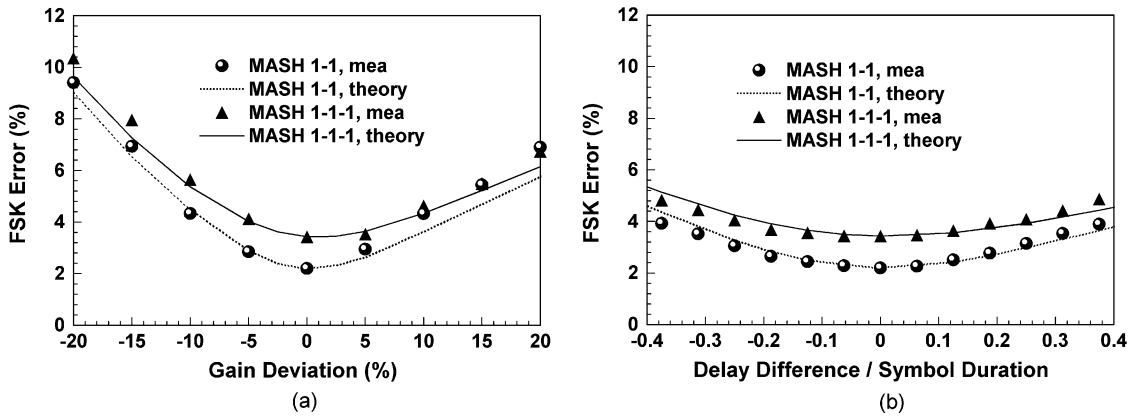


Fig. 11. Calculated and measured FSK errors versus: (a) gain deviation and (b) normalized delay difference for the TPDSM-based GFSK transmitters adopting different MASH designs and 100 kHz for the PLL bandwidth.

Figs. 6 and 7 show the comparison between the simulated and measured phase noises for the output carriers of the fractional- N synthesizer with the PLL bandwidth designed at 25 and 100 kHz, respectively. The comparisons show very good agreement. In the offset frequencies lower than the PLL bandwidth, the MASH 1-1 design has lower carrier phase noise than the MASH 1-1-1 design by approximately 5–8 dB. This is because $\phi_{n,\text{REF}}$ and $\phi_{n,\text{DSM}}$ in (9) contribute primarily to such a PLL in-band phase noise where the latter in the MASH 1-1 de-

sign is lower by approximately 10 dB than in the MASH 1-1-1 design, as simulated in Fig. 3.

With the measured phase noises of output carriers, as shown in Figs. 6 and 7, we can evaluate $\Delta f_{n,\text{rms}}$ according to (21) as a function of the data rate, and subsequently the corresponding FSK error from (20) as the ratio of $\Delta f_{n,\text{rms}}$ to Δf_{avg} under the two-point match condition ($\Delta f_{\text{sig,std}} = 0$). The results for the MASH 1-1 design are shown in Fig. 8. It is noted that both $\Delta f_{n,\text{rms}}$ and Δf_{avg} increase with data rate, which results in a

peak FSK error at a certain data rate. Except for very low data rates, the case with the lower PLL bandwidth exhibits a lower Δf_{n_rms} , and corresponds to a lower FSK error. For our targeted system application, the measurement data for FSK errors have been taken at a 2.5-Mb/s data rate under the two-point match condition, and are found to be in very good agreement with our theoretical predictions. For another application to a Bluetooth transmitter with a data rate set at 1 Mb/s [3], the agreement is also excellent.

Figs. 9 and 10 show the comparison between the theoretical and measured results of the averaged frequency deviation and FSK error, respectively, for the transmitter adopting the MASH 1-1 design. Both parameters are shown as functions of gain deviation and delay difference in consideration of the different PLL bandwidth. One can see that our theoretical predictions agree quite well with the measured results in the comparisons of both parameters. A larger gain deviation or delay difference causes more offset of frequency deviation from its default value, i.e., 390 kHz, as seen in Fig. 9, and also increases the FSK errors, as seen in Fig. 10. The effects of the PLL bandwidth on both parameters behave quite differently. From Fig. 9, the PLL bandwidth has little influence on the averaged frequency deviation. However, from Fig. 10, a larger PLL bandwidth increases not only the FSK errors, but also the sensitivity of FSK errors due to the two-point mismatch factors. Fig. 11(a) and (b) shows the comparison between the theoretical and measured FSK errors when shown as function of gain deviation and delay difference, respectively, in consideration of the different MASH designs. It is noted that the PLL bandwidth is fixed at 100 kHz for this case. As expected, the MASH 1-1 design corresponds to a lower FSK error due to a smaller nonlinear intermodulation noise. The good agreement between simulation and measurement in Fig. 11 has verified that our theory can predict the combined effects due to the PLL nonlinearity and two-point mismatches quite successfully.

Since a larger PLL bandwidth is generally beneficial to the decrease of the PLL stable time, a tradeoff has to be made between the PLL stable time and modulation accuracy at the choice of PLL bandwidth in a practical design. For example, in our particular design for the applications to a high-performance 2.4-GHz FHSS system, the TPDSM-based GFSK transmitter adopts the MASH 1-1 scheme and selects the PLL bandwidth at 100 kHz. The final specifications include a variable data rate up to 2.5 Mb/s, a PLL stable time less than 15 μ s, and an FSK error as low as 2.2% after minimizing the two-point mismatches.

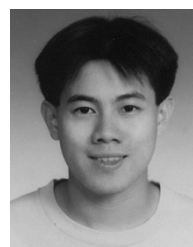
IV. CONCLUSION

A theoretical approach for designing high-performance FH RF transmitters based on a TPDSM architecture has been presented. The proposed methodology can help us to optimize the transmitter performance by means of choosing the right PLL bandwidth and MASH order in conjunction with minimizing the two-point mismatches. In our study, a 2.4-GHz TPDSM-based GFSK transmitter has been implemented with a data rate up to 2.5 Mb/s and PLL stable time less than 15 μ s by following the design methodology. The performance is outstanding when

compared to the current Bluetooth products with specifications for a data rate up to 1 Mb/s and PLL stable time less than 220 μ s. In addition, all theoretical predictions in the design stage agree quite well with the final measured results. Such a success in design results from an accurate system analysis that well predicts the combined effects due to the PLL nonlinearity and two-point mismatches in a TPDSM architecture.

REFERENCES

- [1] R. A. Meyers and P. H. Waters, "Synthesizer review for pan-European digital cellular radio," in *Proc. IEEE VLSI Implementations for Second Generation Digital Cordless and Mobile Telecommunication Systems Colloq.*, 1990, pp. 8/1–8/8.
- [2] C. Durdodt, M. Friedrich, C. Grewing, M. Hammes, A. Hanke, S. Heinen, J. Oehm, D. Pham-Stabner, D. Seippel, D. Theil, S. V. Waasen, and E. Wagner, "A low-IF RX two-point $\Delta\Sigma$ -modulation TX CMOS single-chip Bluetooth solution," *IEEE Trans. Microwave Theory Tech.*, vol. 49, pp. 1531–1537, Sept. 2001.
- [3] K. C. Peng, C. H. Huang, C. N. Pan, and T. S. Horng, "High-performance Bluetooth transmitters using two-point delta-sigma modulation," *Electron. Lett.*, vol. 40, pp. 544–545, Apr. 2004.
- [4] J. Gilb, "Bluetooth radio architectures," in *IEEE Radio Frequency Integrated Circuit Symp. Dig.*, 2000, pp. 3–6.
- [5] C. O'Keeffe and M. Fitzgibbon, "A direct digital modulation technique for GSM/PCS/DCS applications using a 24 bit multi-accumulator fractional- N synthesizer," in *IEE Systems on a Chip Workshop Dig.*, 2000, pp. 6/1–6/11.
- [6] K. C. Peng, J. K. Jau, and T. S. Horng, "A novel EER transmitter using two-point delta-sigma modulation scheme for WLAN and 3G applications," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2002, pp. 1651–1654.
- [7] B. De Muer and M. Steyaert, "On the analysis of $\Delta\Sigma$ fractional- N frequency synthesizers for high-spectral purity," *IEEE J. Solid-State Circuits*, vol. 50, pp. 784–793, Nov. 2003.
- [8] K. C. Peng, C. H. Huang, C. N. Pan, and T. S. Horng, "High performance frequency hopping transmitters using two-point delta-sigma modulation," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2004, pp. 2011–2014.
- [9] B. Miller and R. Conley, "A multiple modulator fractional divider," *IEEE Trans. Instrum. Meas.*, vol. 40, pp. 578–583, June 1991.
- [10] *HP 89440A/HP 89441A Operator's Guide*, Hewlett-Packard Company, Palo Alto, CA, 1996.
- [11] *Fundamentals of Spectrum Analysis*, 1st ed. Munich, Germany: Rohde & Schwarz, 2001, pp. 119–125.



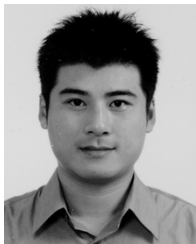
Kang-Chun Peng (S'00) was born February 18, 1976, in Taipei, Taiwan, R.O.C. He received the B.S.E.E. and M.S.E.E. degrees from the National Sun Yat-Sen University, Kaohsiung, Taiwan, R.O.C., in 1998 and 2000, respectively, and is currently working toward the Ph.D. degree in electrical engineering at the National Sun Yat-Sen University.

His main research interests are fractional- N frequency synthesizers, modulated frequency synthesizers, and advanced RF transceiver architectures for wireless personal area network (WPAN).



Chien-Hsiang Huang was born August 24, 1978, in Kaohsiung, Taiwan, R.O.C. He received the B.S.E.E. and M.S.E.E. degrees from the National Sun Yat-Sen University, Kaohsiung, Taiwan, R.O.C., in 2000 and 2002, respectively, and is currently working toward the Ph.D. degree in electrical engineering at the National Sun Yat-Sen University.

His main research interests are wide-band VCOs and frequency synthesizers for digital video broadcasting (DVB).



Chien-Jung Li was born October 26, 1979, in Tainan, Taiwan, R.O.C. He received the B.S.E.E. degree from the National Sun Yat-Sen University, Kaohsiung, Taiwan, R.O.C., in 2002, and is currently working toward the Ph.D. degree in electrical engineering at the National Sun Yat-Sen University.

His main research interests are integrated-circuit development of frequency synthesizers.



Tzyy-Sheng Horng (S'88–M'92) was born December 7, 1963, in Taichung, Taiwan, R.O.C. He received the B.S.E.E. degree from the National Taiwan University, Taipei, Taiwan, R.O.C., in 1985, and the M.S.E.E. and Ph.D. degrees from the University of California at Los Angeles, in 1990 and 1992, respectively.

He is currently a Professor with the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan, R.O.C. His research interests are in the areas of RF and microwave

integrated circuits and packages.