Electrical Performance Improvements on RFICs Using Bump Chip Carrier Packages as Compared to Standard Thin Shrink Small Outline Packages

Tzyy-Sheng Horng, *Member, IEEE*, Sung-Mao Wu, Chi-Tsung Chiu, and Chih-Pin Hung

***Abstract*—The electrical models of bump chip carrier (BCC) packages have been established based on the S-parameter measurement. When compared to the standard thin shrink small outline packages (TSSOPs), BCC packages show much smaller parasitics in the equivalent model. In the simulation, the insertion and return losses for a packaged 50-Ω microstrip line are calculated against frequency. BCC packages are also less lossy than TSSOPs over a wide frequency range. By setting a random variable with Gaussian distribution varied within a certain range for each equivalent circuit element of the packages, the Monte Carlo analysis has been performed to study the package effects on a gaas heterojunction bipolar transistor (HBT). Again, BCC packages cause less decrement of HBTs unity-gain bandwidth than TSSOPs.**

***Index Terms*—Bump chip carrier packages, heterojunction bipolar transistors, Monte Carlo analysis, RFIC packages, think shrink small outline packages.**

I. Introduction

BCC package is one type of chip scale packages (CSP), which can provide the smaller space advantages over the conventional leaded small outline packages [1]–[3]. With ease of attachment to the printed circuit board (PCB), it is also cost-effective in surface mount assembly when compared to the other CSPs like micro ball grid arrays. Fig. 1 shows an electrically and thermally enhanced BCC (abbreviated as BCC^{++}) package. As seen from the cross-sectional sketch in Fig. 1, a resin package sealing the semiconductor chip has protrusions covered with metal on the backside to form the basin-like center pad and a number of 16 I/O pads around the center pad. Electrical connection between the chip and the I/O pads relies on the bondwires only and such a leadless configuration can achieve a substantial decrease in package inductance. In addition, the center pad can be attached directly to PCB and thus provide excellent thermal spread and ground shield. In comparison with the 16-lead TSSOP, one of the currently popular radio-frequency integrated circuit (RFIC) packages, the 16-pad BCC^{++} package is only one-half in area and has been estimated to reduce the thermal resistance as well as the package inductance by more than 40%.

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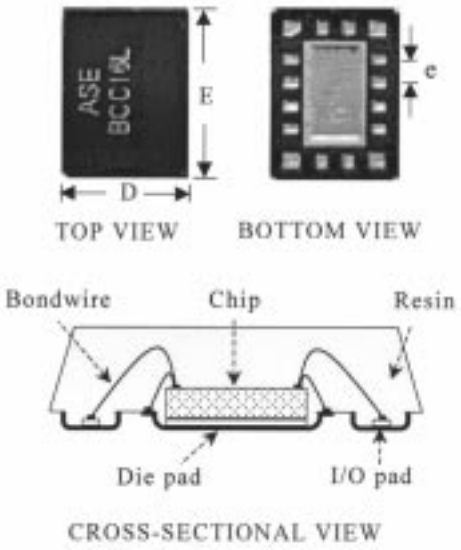

Fig. 1. Top, bottom, and cross-sectional views of a 16-pad BCC^{++} package.

To distinguish the difference of the package effects on RFICs between BCC packages and TSSOPs, this research has been devoted to direct extraction of the electrical models at radio frequencies from the measured S-parameters of the package terminals in a variety of wire-bonding diagrams[4]–[6]. Fundamental RF parameters such as insertion and return losses can be further found from the extracted package models. When applied to RFICs, these RF parameters can offer excellent insight into the degradation of gain, bandwidth, and stability due to the package parasitics.

Among the microwave and millimeter-wave applications, the GaAs HBT is a promising candidate for power amplification [7], [8]. Recently, the GaAs HBT power amplifiers have been widely used in modern mobile communications for its merits of high efficiency and linearity, small size and single voltage operation. However, circuit design of such component is a challenging task due to HBT's sensitive electrothermal characteristics. Conventional design uses the chip-on-board technique to exclude the package effects but increases the cost of assembly. An intention of this research is to explore the potential capability of the BCC packages applied to HBTs. With superior electrical and thermal performance, BCC packages may take an advantageous position in the packaging of the HBT products in the near future.

II. Modeling Techniques

Fig. 2 shows the equipment set-up for measuring a 16-pad BCC^{++} package. When seen from the bottom side of the

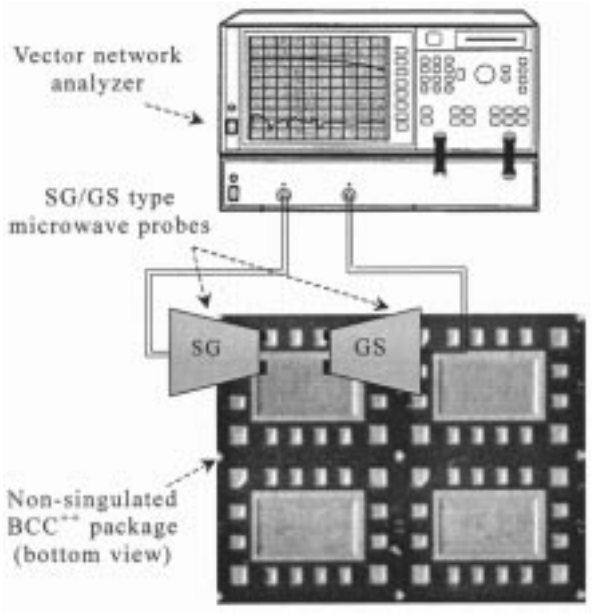

Fig. 2. Fixture-free measurement set-up for electrical modeling of the 16-pad BCC^{++} package.

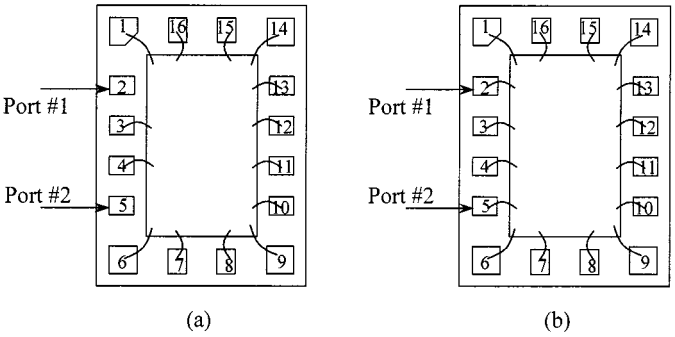

Fig. 3. (a) Open-path and (b) short-path wire-bonding diagrams in the 16-pad BCC^{++} package.

package, the big center die pad used for grounding and the other signal pads around it are in a coplanar configuration such that they can be measured by a vector network analyzer through a pair of fixed-pitch signal-ground (SG) and ground-signal (GS) type microwave probes. Therefore, there is no need to design the PCB fixture as required for grounding parts of the leads in measuring TSSOPs [5], [6]. This saves a great effort to calibrate the fixture parasitics. The package samples for electrical modeling include the open-path and short-path configurations, as shown in Fig. 3. In the open-path configuration, the signal pads under test are left open-ended while the other pads are all wire-bonded to the rim of the die pad. For the short-path configuration, the pads under test will be wire-bonded to the rim of the die pad as well.

As examples, Fig. 4(a)–(c) show the measured two-port S-parameters between the pads (3,4), (2,16), and (2,5) respectively for both open-path and short-path configurations in the 16-pad BCC^{++} package. To account for the pad parasitics in the open-path configuration, an equivalent π model composed of three capacitances as shown in Fig. 5(a) has been used. In the extraction, the measured scattering matrix $([S]^{\mathrm{op}})$ is

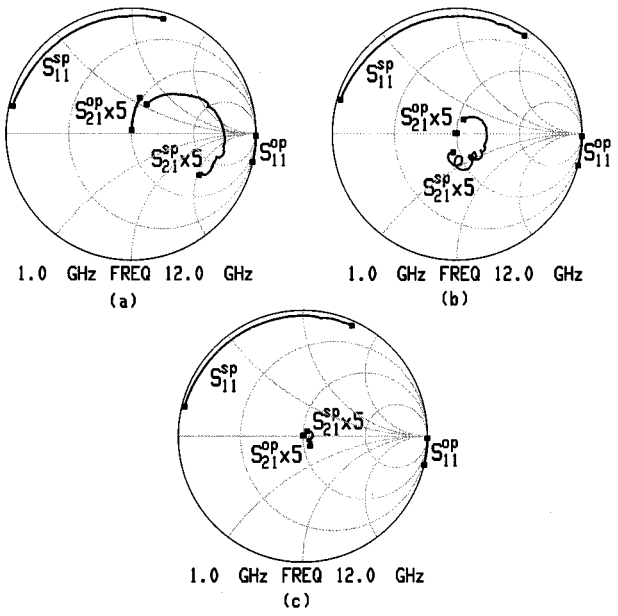

Fig. 4. Measured two-port S-parameters between the pads (a) (3,4), (b) (2,16), and (c) (2,5) in the 16-pad BCC^{++} package.

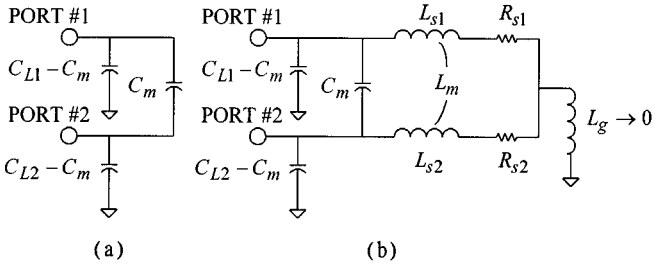

Fig. 5. Equivalent circuit of the (a) open-path and (b) short-path configuration in the 16-pad BCC^{++} package.

converted into the admittance matrix $([Y]^{\mathrm{op}})$ from which the corresponding loaded and mutual capacitances can be found as

$$[Y]^{\mathrm{op}} = Z_0^{-1}([U]+[S]^{\mathrm{op}})^{-1}([U]-[S]^{\mathrm{op}}) \tag{1}$$

$$C_{L1} = \frac{\mathrm{Im}\,(Y_{11}^{\mathrm{op}})}{2\pi f} \tag{2}$$

$$C_{L2} = \frac{\mathrm{Im}\,(Y_{22}^{\mathrm{op}})}{2\pi f} \tag{3}$$

$$C_m = -\frac{\mathrm{Im}\,(Y_{12}^{\mathrm{op}})}{2\pi f} \tag{4}$$

where $Z_0 = 50\,\Omega$ is the impedance of this measurement system and $[U]$ is an identity matrix. The curves of extracted quantities are plotted in Fig. 6. The quantity of individual loaded capacitance depends on the pad size and ranges from 25 fF to 35 fF typically. The mutual capacitance for the adjacent pads is about 9 fF and approaches almost zero for the nonadjacent pads. In the short-path configuration, except the same π model of three capacitances in the front, two lossy inductances with mutual terms are included to account for the bond-wire parasitics, as shown in Fig. 5(b). The measured scattering matrix $([S]^{\mathrm{sp}})$ is first converted into the admittance matrix $([Y]^{\mathrm{sp}})$. After subtracting the admittance matrix $([Y]^{\mathrm{op}})$ contributed from the pad parasitics,

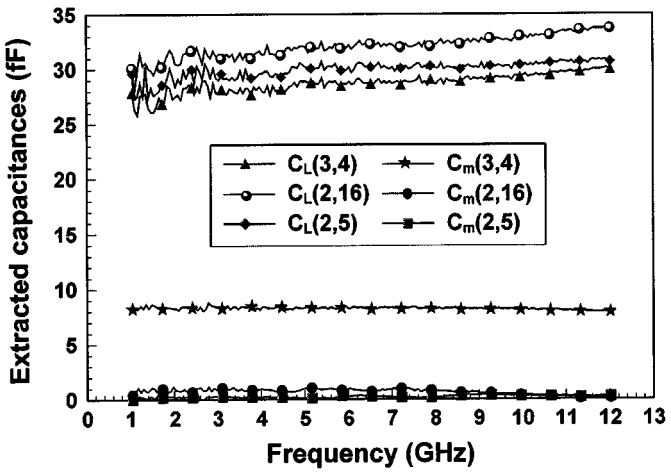

Fig. 6. Extracted quantities of loaded and mutual capacitances in the equivalent circuit of the 16-pad BCC^{++} package.

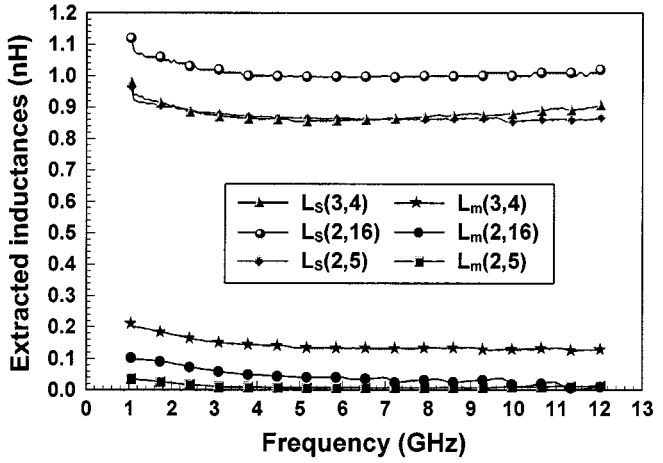

Fig. 7. Extracted quantities of self and mutual inductances in the equivalent circuit of the 16-pad BCC^{++} package.

we convert the admittance matrix into the impedance matrix from which the corresponding self and mutual inductances as well as the series resistances can be found as

$$[Y]^{\mathrm{sp}} = \left(Z_0^{-1}([U]+[S]^{\mathrm{sp}})^{-1}([U]-[S]^{\mathrm{sp}})\right) \tag{5}$$

$$[Z]^{\mathrm{sp}} = ([Y]^{\mathrm{sp}} - [Y]^{\mathrm{op}})^{-1} \tag{6}$$

$$L_{s1} = \frac{\mathrm{Im}(Z_{11}^{\mathrm{sp}})}{2\pi f} \tag{7}$$

$$L_{s2} = \frac{\mathrm{Im}(Z_{22}^{\mathrm{sp}})}{2\pi f} \tag{8}$$

$$L_m = \frac{\mathrm{Im}(Z_{12}^{\mathrm{sp}})}{2\pi f} \tag{9}$$

$$R_{s1} = \mathrm{Re}(Z_{11}^{\mathrm{sp}}) \tag{10}$$

$$R_{s2} = \mathrm{Re}(Z_{22}^{\mathrm{sp}}). \tag{11}$$

Note that extraction of self and mutual inductances using (7)–(9) is under an assumption of zero ground inductance, which can be accepted as true for the 16-pad BCC^{++} package. However, the same assumption is not good for the TSSOP packages. Thus, measurement of the ground inductance becomes necessary for TSSOPs [5], [6]. It is also noted that we have omitted the bondwire capacitance because in the short-path configuration the bondwire is attached to ground (die pad) with the slightest capacitive effect. When connected to a real RFIC device with a typical impedance as low as 50 Ω, the influence due to bondwire capacitance is still not evident and can be ignored.

As a result, Figs. 7 and 8 show the extracted quantities of inductances and resistances respectively. The quantity of individual self inductance depends on the bondwire length and ranges from 0.75 nH to 1.35 nH typically. The mutual inductance reaches its upper limit about 0.17 nH for the adjacent pads and decreases quite quickly for the nonadjacent pads. One can observe that the extracted inductance and capacitance quantities in Figs. 6 and 7 have only slight dependence on frequency from 1 to 12 GHz. However, in Fig. 8 the extracted resistance curves exhibit a much closer frequency dependence. Their behavior can be explained by the losses due to the conductor skin effects and dielectric leakage. Both losses increase with frequency.

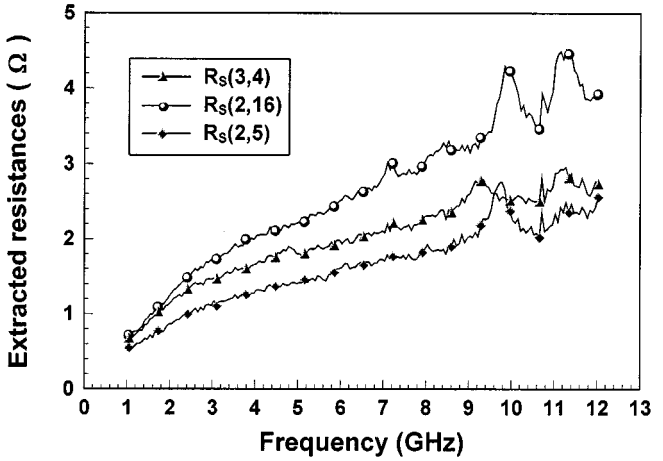

Fig. 8. Extracted quantities of series resistances in the equivalent circuit of the 16-pad BCC^{++} package.

III. Insertion and Return Losses of Packaged Microstrip Lines

Insertion and return losses are important parameters for evaluating the RFIC packages. Fig. 9 shows an arbitrary pair of the pads in a 16-pad BCC^{++} package that connect a 50-Ω microstrip line on a 100 μm thick GaAs substrate through the bondwires. The corresponding width for such a 50-Ω line is 73 μm. In the simulation it is assumed that the line is lossless and the shunt capacitances for the bond pads on the substrate are negligible. For the following cases to be presented, the pads (3, 4), (2, 16), and (2, 5) are assumed to connect the microstrip line with a variable length equal to e, $2e$, and $3e$ respectively. Note that e denotes the pad pitch, which is 0.65 mm for the 16-pad BCC^{++} package. An equivalent circuit of Fig. 9 is shown in Fig. 10 and its scattering matrix $([S]^l)$ can be derived as

$$[Z]^l = [Z]^{\mathrm{sp}} + [Z]^{\mathrm{line}} \tag{12}$$

$$[Y]^l = ([Z]^l)^{-1} + [Y]^{\mathrm{op}} \tag{13}$$

$$[S]^l = (Z_0^{-1}[U] + [Y]^l)^{-1}(Z_0^{-1}[U] - [Y]^l) \tag{14}$$

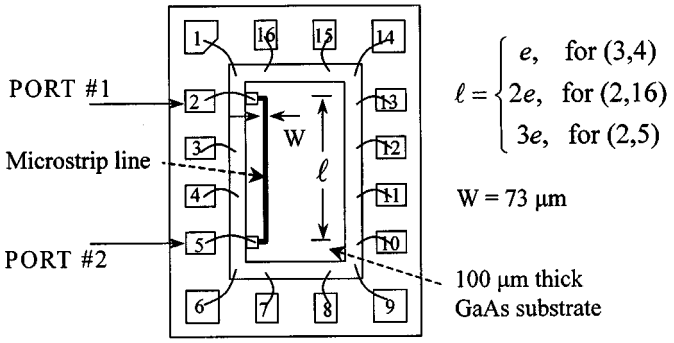

Fig. 9. Arbitrary pair of the pads in a 16-pad BCC^{++} package connecting an on-chip 50-Ω microstrip line through bondwires.

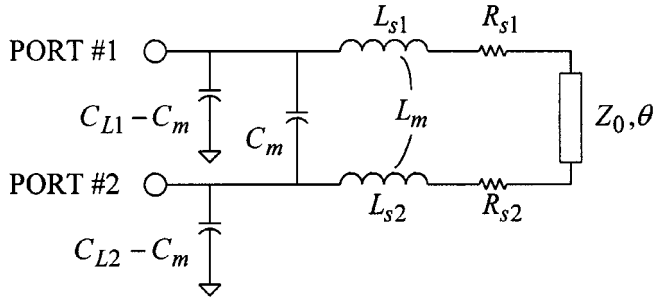

Fig. 10. Equivalent circuit of Fig. 9.

where

$$[Z]^{\text{line}} = \begin{bmatrix} -jZ_0\cot\theta & -jZ_0\csc\theta \\ -jZ_0\csc\theta & -jZ_0\cot\theta \end{bmatrix} \tag{15}$$

and

$$\theta = \frac{2\pi f l\sqrt{\epsilon_{\text{eff}}}}{c}. \tag{16}$$

Note that $[Z]^{\text{line}}$ represents the impedance matrix of a lossless microstrip line with an effective dielectric constant $\epsilon_{\text{eff}} = 8.33$.

The simulated insertion and return losses are shown in Figs. 11 and 12, respectively. Generally speaking, the equivalent loop inductance dominates the insertion and return losses at low frequencies. From Fig. 7, the sequence from the smallest to the largest series inductance is $(3,4) < (2,5) < (2,16)$ while the sequence from the smallest to the largest mutual inductance is $(2,5) < (2,16) < (3,4)$. This results in an equivalent loop inductance whose quantity follows the sequence $(3,4) < (2,5) < (2,16)$, which can explain the behavior for the insertion and return losses in Figs. 11 and 12 up to 4.7 GHz effectively. Above a certain frequency each insertion-loss resposne will generally have an overshoot then followed by the cut off. A five-section stepped impedance low-pass filter can explain this. The pads as well as the 50-Ω microstrip line can be regarded as relatively low impedance lines while the bondwires can be regarded as relatively high-impedance lines. As a result, an equivalent fifth order low-pass filter causes such a phenomenon. It has been found that the longer the microstrip line is, the lower the cut-off frequency will result.

For comparison with the 16-lead TSSOP, we simulate the insertion and return losses for the three different pairs of leads

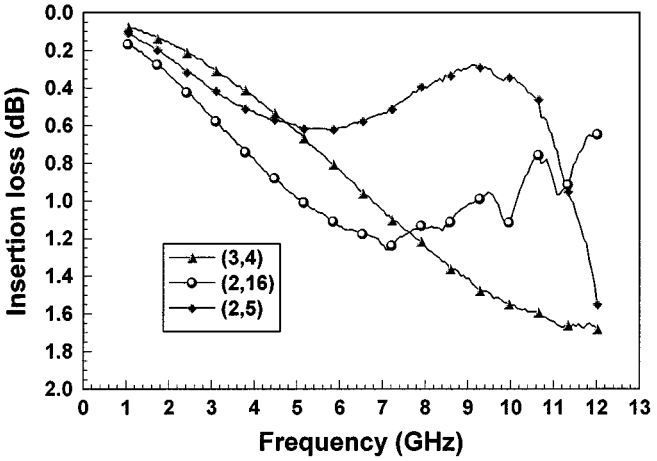

Fig. 11. The simulated insertion losses against frequency for the configuration of Fig. 9.

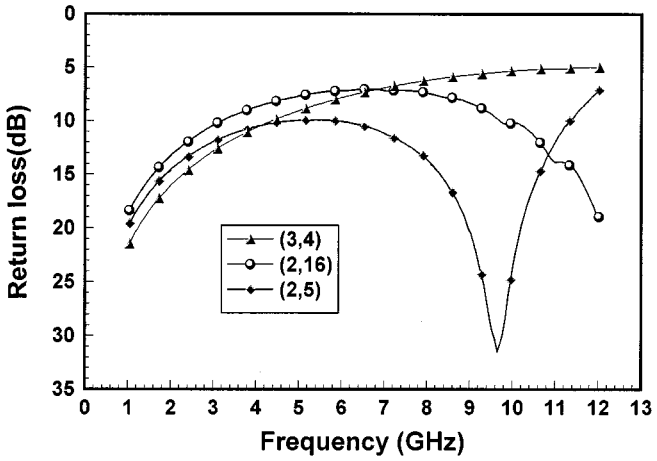

Fig. 12. Simulated return losses against frequency for the configuration of Fig. 9.

(4,5), (1,2), and (3,6) connecting the identical microstrip line with length equal to e, $2e$, and $3e$, respectively, as illustrated in Fig. 13. Note that the 16-lead TSSOP has the same pitch $(e = 0.65$ mm$)$ as the 16-pad BCC^{++} package. Extraction of the coupled-lead models for the 16-pad TSSOP has been done in our previous works [5], [6]. As a result, the calculated insertion and return losses against frequency are plotted in Figs. 14 and 15 respectively. It was found that similar explanations on the basis of equivalent loop inductance and low-pass filter effects are still applicable. When connecting the microstrip line of equal length, the 16-lead TSSOP has higher insertion loss or lower return loss than the 16-pad BCC^{++} package at low frequencies. In addition, the 16-lead TSSOP has lower cut-off frequency, and thus shows more attenuation at high frequencies.

IV. Monte Carlo Analysis of Packaged HBTs

Based on the S-parameters simulated using Ansoft's HFSS and verified in part by measurements, inTables I and II we summarize the range of extracted quantities of equivalent circuit elements for the BCC package and TSSOP, respectively, with an I/O count of 8, 16, 20, and 24. Compared to each TSSOP having the same I/O count individually, the BCC package reduces self

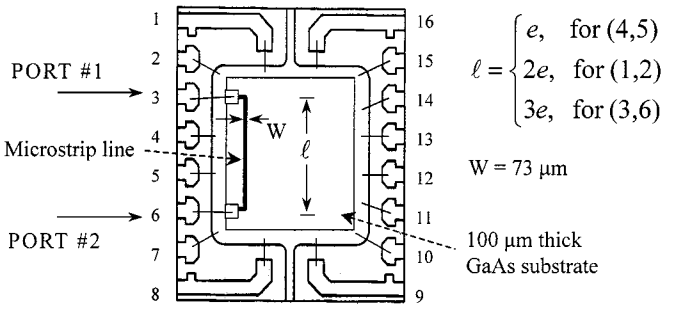

Fig. 13. Arbitrary pair of the leads in a 16-lead TSSOP connecting an on-chip 50-Ω microstrip line through bondwires.

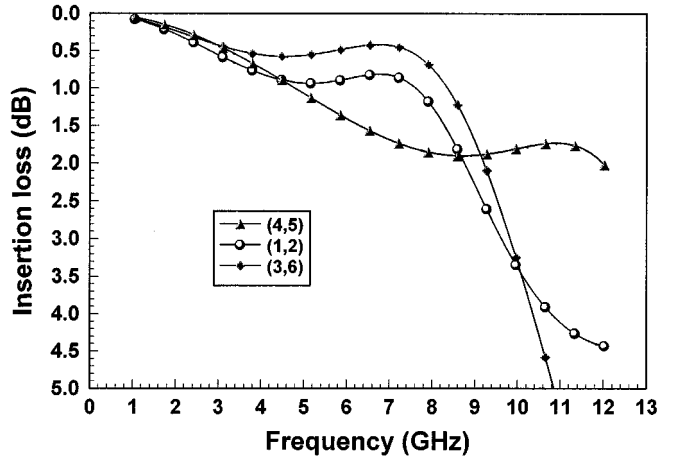

Fig. 14. Simulated insertion losses against frequency for the configuration of Fig. 13.

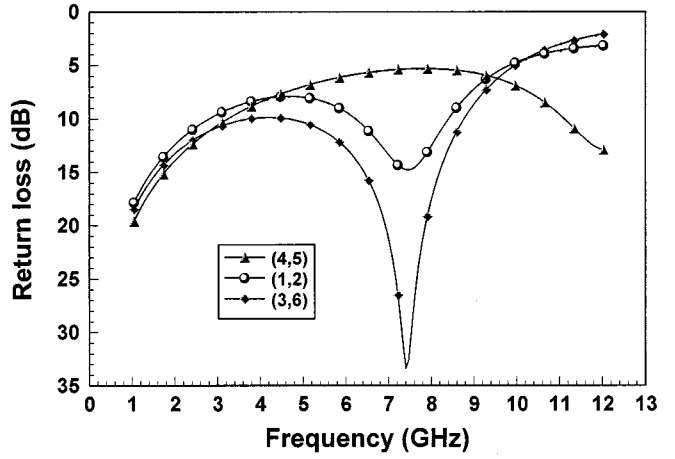

Fig. 15. Simulated return losses against frequency for the configuration of Fig. 13.

and mutual inductances by more than 40% as well as loaded and mutual capacitances by more than 80% in average. In addition, each BCC package has negligible ground inductance while each TSSOP has that quantity within 0.1–0.25 nH. It is therefore reasonable to conclude that the BCC packages are electrically superior to TSSOPs. For modeling the bondwires and leads, the frequency-dependent losses will generally lead to the frequency dependence of the resistances in an equivalent series or parallel LR circuit shown in Fig. 16. To become a qualified spice model,

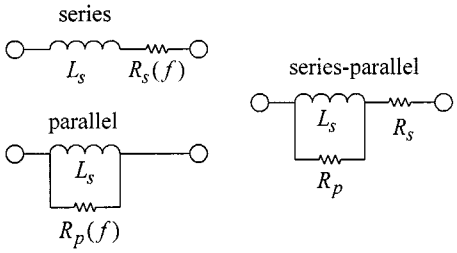

Fig. 16. Series, parallel and series—parallel LR circuits for modelling the frequency—dependent losses.

TABLE I
RANGE OF THE EXTRACTED QUANTITIES OF THE EQUIVALENT CIRCUIT ELEMENTS IN THE BCC PACKAGES

Package type	8-pad BCC^{++}	16-pad BCC^{++}	20-pad BCC^{++}	24-pad BCC^{++}
E (mm)	3.8	4.55	5.2	4.0
D (mm)	2.8	3.4	4.2	4.0
e (mm)	0.5	0.65	0.65	0.5
L_S (nH)	0.75~1.35	0.75~1.35	0.75~1.35	0.75~1.35
C_L (pF)	0.025~0.035	0.025~0.035	0.025~0.035	0.025~0.035
L_m (nH)	0.02~0.18	0~0.17	0~0.17	0~0.18
C_m (pF)	0~0.01	0~0.009	0~0.009	0~0.01
R_s (OH)	0.55~0.75	0.55~0.75	0.55~0.75	0.55~0.75
R_p (KOH)	1.2~1.7	1.2~1.7	1.2~1.7	1.2~1.7
L_g (nH)	≒0	≒0	≒0	≒0

TABLE II
RANGE OF THE EXTRACTED QUANTITIES OF THE EQUIVALENT CIRCUIT ELEMENTS IN THE TSSOP PACKAGES

Package type	8-lead TSSOP	16-lead TSSOP	20-lead TSSOP	24-lead TSSOP
E (mm)	6.4	6.4	6.4	6.4
D (mm)	3.0	5.0	6.5	7.8
e (mm)	0.65	0.65	0.65	0.65
L_S (nH)	1.35~1.4	1.57~2.11	1.59~2.06	1.52~2.24
C_L (pF)	0.17~0.18	0.17~0.24	0.17~0.24	0.17~0.26
L_m (nH)	0.04~0.24	0.01~0.44	0.01~0.44	0.01~0.48
C_m (pF)	0~0.06	0~0.07	0~0.07	0~0.09
R_s (OH)	0.4~0.6	0.6~0.8	0.6~0.8	0.6~0.9
R_p (KOH)	0.8~1	1.2~1.7	1.3~1.6	1.2~1.8
L_g (nH)	0.1~0.2	0.1~0.2	0.1~0.2	0.1~0.25

a series–parallel LR model is used instead, as also shown in Fig. 16. Within a certain bandwidth the series resistance R_s is determined by the quantity extracted from a series LR model at the lowest frequency while the parallel resistance R_p is determined by the quantity extracted from a parallel LR model at the highest frequency. The range of extracted R_s and R_p in a series–parallel LR model for both BCCs and TSSOPs is also listed in Tables I and II. Unlike capacitances and inductances, BCC packages are short of a pronounced reduction of both resistances when compared to TSSOPs.

In the applications to RFICs, we simulate the gain responses of a GaAs HBT in consideration of the package effects. Fig. 17

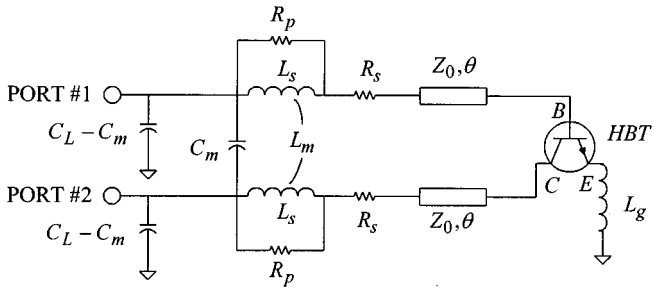

Fig. 17. Equivalent circuit for simulating a packaged HBT.

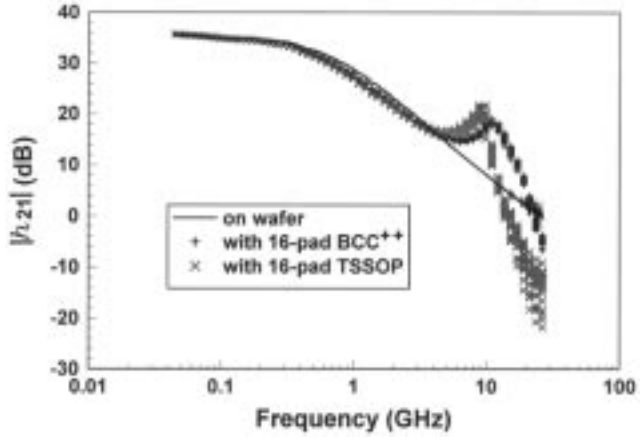

Fig. 18. Simulated short-circuit current gain of the packaged HBT against frequency.

shows the equivalent circuit in simulation for an arbitrary pair of BCC package pads that connect a GaAs HBT through two sections of one-pitch long 50-Ω microstrip lines and bondwires. The HBT has an emitter size of 60 μm^2 and is treated as a unit cell for power amplification. With the bias conditions, $V_{ce} = 3$ V and $I_c = 6$ mA, the measured S-parameters can be used to calculate the corresponding short-circuit current gain given as

$$h_{21} = \frac{2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}. \tag{17}$$

When measured on the wafer, the HBT has a magnitude of h_{21} about 60 (35.6 dB) at direct current and a cut-off frequency (f_T) defined as the unity-gain bandwidth of $|h_{21}|$ that approaches 26.5 GHz. By setting a random variable with Gaussian distribution varied within the tabulated range in Tables I and II for each equivalent circuit element, the Monte Carlo analysis has been performed to compare the package effects on the HBT between the 16-pad BCC^{++} package and 16-lead TSSOP with undetermined pin-out assignment. As a result, Fig. 18 shows the simulated $|h_{21}|$ in decibels against frequency in a logarithmic scale. It can be seen that at high frequencies the curves for the packaged HBTs overshoot before a cut off occurs. It is noted that the cut-off phenomena decrease f_T dramatically. Theoretical prediction of f_T for the HBT packaged with the 16-pad BCC^{++} package and 16-lead TSSOP is around 21.5 GHz and 14.5 GHz, respectively. This implies that the 16-lead TSSOP degrades the HBT performance more significantly than the 16-pad BCC^{++} package.

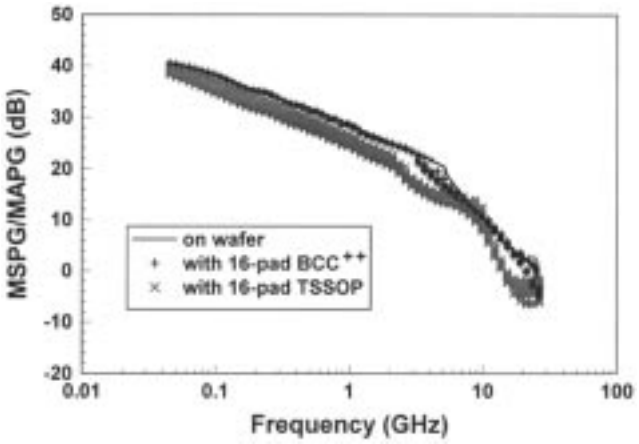

Fig. 19. Simulated maximum stable/available power gain of the packaged HBT against frequency.

Assuming a simultaneous conjugate match for the HBT, we can calculate its maximum available power gain (MAPG) using the expression

$$G_{MA} = \frac{|S_{21}|}{|S_{12}|}\left(K - \sqrt{K^2 - 1}\right) \tag{18}$$

where K is the stability factor defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{19}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}. \tag{20}$$

At relatively low frequencies where an HBT is potentially unstable $(K < 1)$, the maximum stable power gain (MSPG) is used instead of the maximum available power gain. The definition of MSPG is given as

$$G_{MS} = \frac{|S_{21}|}{|S_{12}|}. \tag{21}$$

The results are demonstrated in Fig. 19. It can be seen that the gain roll-off characteristics in the potentially unstable region is 3 dB/octave and the MSPG/MAPG break-point frequency is 5 GHz. In the package effects, two dominant factors are found to cause the reduction of G_{MS} below 5 GHz. One is due to the ground inductance (L_g), the so-called emitter degeneration effect. The other is due to the mutual capacitance (C_m) based on the well-known Miller effect. One can find that the 16-pad BCC^{++} package causes much less gain reduction than the 16-lead TSSOP because the former has much smaller ground inductance and mutual capacitance. Above 5 GHz the HBT is unconditionally stable. The low-pass filter effect due to package plays an important role in this region to cause an overshoot followed by a cut off. In addition to the f_T mentioned above, the maximum oscillation frequency $(f_{\max})$ defined as the unity-gain bandwidth of G_{MA} is another important figure of merit to estimate transistor's high-speed/high-frequency performance. When measured on the wafer, the HBT has a $f_{\max}$ that also approaches 26.5 GHz. However, the cut-off phenomena reduce $f_{\max}$ to 20 GHz and 14 GHz for the HBT packaged with the 16-pad BCC^{++} package and 16-lead TSSOP, respectively. Comparison of both package effects in

Fig. 19 shows that the HBT packaged with the 16-pad BCC^{++} package has a much closer response to the on-wafer HBT.

V. Conclusion

A complete methodology for direct extraction of the equivalent circuit elements of the BCC packages from the measured S-parameters has been developed. The electrical models established are broadband and good for RFIC applications. In comparison with TSSOPs, BCC packages have the advantages of smaller size and parasitics. Simulation of insertion and return losses also demonstrates the electrical superiority of BCC packages to TSSOPs. The Monte Carlo analysis has been applied to evaluate the package effects on a GaAs HBT. Electrical degradation of HBT due to BCC packages is much slighter than TSSOPs.

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