Ultralow Power Injection-Locked GFSK Receiver for Short-Range Wireless Systems

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***Abstract*—This brief presents a novel CMOS Gaussian frequency-shift keying (GFSK) receiver with an ultralow power consumption, which is based on the injection-locking technique for short-range wireless systems. Additionally, through reducing the oscillation current amplitude of the injection-locked oscillator, the GFSK receiver sensitivity is significantly improved. While comprising a submilliwatt low-noise amplifier, a trifilar transformer splitter, and an injection-locked self-oscillating mixer, the proposed receiver is fabricated using a 90-nm CMOS 1P9M technology. Measurement results indicate a sensitivity of −81 dBm, with a power consumption of 1.8 mW, when a Bluetooth GFSK signal with a data rate of 1 Mb/s is received.**

***Index Terms*—CMOS Gaussian frequency-shift keying (GFSK) receiver, injection-locked receiver, self-oscillating mixer (SOM), trifilar transformer splitter.**

I. Introduction

SHORT-RANGE wireless (SRW) systems, including wireless sensor networks and wireless body area networks, have attracted increasing attention in recent years for their potential use in a diverse array of applications, including health monitoring and positioning and ranging. However, sensor devices in these systems require a low-power RF receiver with a high sensitivity because the RF receiver often consumes most of the available battery power.

A Gaussian frequency-shift keying (GFSK) modulation scheme is widely used in wireless communications such as Bluetooth because its constant envelope property allows for its use with high-efficiency nonlinear amplifiers without signal distortion. Additionally, noncoherent detection can eliminate the need for power-hungry carrier recovery circuitry. Several injection-locked receivers developed include the amplitude-shift keying [1] and frequency-shift keying (FSK) receivers [2], [3], in which removing the phase-locked loops (PLLs) reduces power consumption. Additionally, low-power short-range gigabit communication systems have been constructed by using the wide locking range of the injection-locked oscillator (ILO) at high injection power [1], [2]. However, despite their potential for ultralow power consumption, injection-locked receivers generally incur poor sensitivity owing to the minimum injection-locking power that depends on the quality factor and oscillation current amplitude of ILOs.

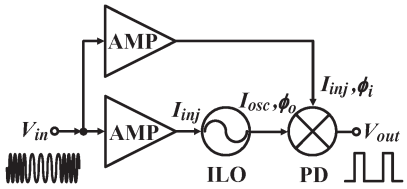

Fig. 1. Conventional injection-locked FSK receiver architecture.

This brief proposes a novel GFSK receiver based on an injection-locked self-oscillating mixer (SOM) to provide low minimum injection-locking power and low power consumption. Moreover, with the assistance of a submilliwatt low-noise amplifier (LNA) and a trifilar transformer splitter, superior receiver sensitivity is achieved.

II. Circuit Analysis

A. ILO-Based Receiver Architecture

For demodulating a GFSK signal, the ILO, which provides a stable phase difference between the injected and output signals, is widely used to achieve a frequency-to-phase conversion [2], [3]. Fig. 1 shows a conventional architecture of an FSK receiver using an ILO [3]. The phase difference detected at the output is given by [4]

$$(\phi_i - \phi_o) \approx \sin^{-1}\left(\frac{\omega_o - \omega_{\rm inj}}{\omega_{\rm LR}}\right) \tag{1}$$

where $\omega_{\rm LR} = (\omega_o I_{\rm inj})/(2QI_{\rm osc})$ is the locking range of the ILO with a quality factor Q, $I_{\rm inj}$ is the injected current amplitude from the received signal $V_{\rm in}$, $I_{\rm osc}$ is the oscillation current amplitude of the ILO, ω_o is the free-running frequency of the ILO, and $\omega_{\rm inj}$ is the frequency of $V_{\rm in}$. In Fig. 1, the output voltage at the phase detector (PD) is given by $V_{\rm out} = k_c\ (\phi_i - \phi_o)$, where k_c is the combined gain of the receiver. This finding implies that $V_{\rm out}$ is low when $\omega_{\rm inj}$ exceeds ω_o; otherwise, it is high. Thus, the combined use of an ILO and a PD achieves a frequency-to-amplitude conversion. Moreover, the locking range of the ILO determines the demodulation bandwidth. Intuitively, a wide locking range can be achieved by significantly reducing the Q-factor of the ILO. However, this procedure poses a high $I_{\rm osc}$ to compensate for the low-Q effect on the oscillation start-up condition. Consequently, $I_{\rm inj}$ dominates the locking range. Thus, as in [1]–[3], conventional

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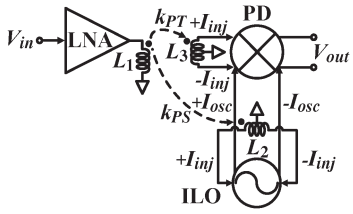

Fig. 2. Proposed injection-locked FSK receiver architecture.

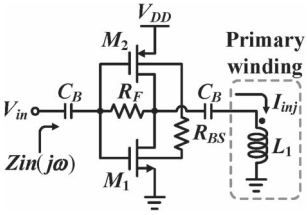

Fig. 3. Circuit schematic of the submilliwatt LNA.

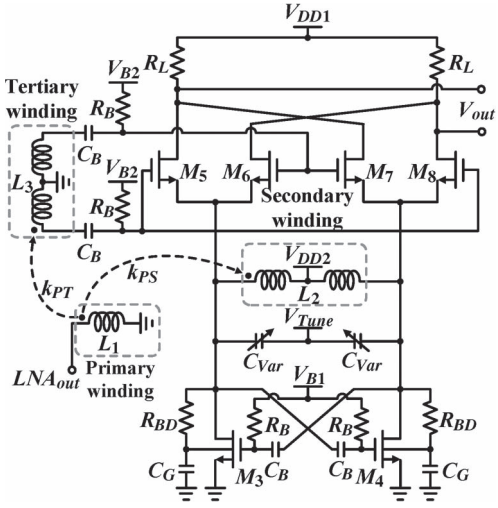

Fig. 4. Circuit schematic of the SOM with a trifilar transformer splitter feed.

injection-locked receivers trade off sensitivity for an increased demodulation bandwidth. However, this design strategy fails to provide the required high sensitivity (i.e., a low $I_{\rm inj}$) for SRW applications.

Conversely, this work examines the feasibility of obtaining a sufficiently large locking range at a low $I_{\rm inj}$ by lowering $I_{\rm osc}$ as much as possible under a stable oscillation condition. Furthermore, as depicted in Fig. 2, a low-power LNA amplifies the received FSK-modulated signal, and its output signal is input to the ILO and the Gilbert-cell switching stage through a trifilar transformer splitter. Notably, the trifilar transformer splitter consists of primary winding inductance L_1, secondary winding inductance L_2, and tertiary winding inductance L_3. The low-power LNA combined with the trifilar transformer splitter, in the proposed configuration, substitutes for the two amplifiers (AMPs) in the configuration in Fig. 1 for reducing the power consumption. Meanwhile, the secondary winding inductance L_2 serves as a tank inductance in the ILO.

B. Submilliwatt LNA

Fig. 3 schematically depicts the submilliwatt LNA with current reuse. Under a given bias current, the adopted complementary topology provides a sufficiently high gain because its equivalent transconductance g_m is twice that of a single common-source transistor. Hence, the power consumption of the LNA can be effectively diminished for a given gain. Additionally, supply voltage V_{DD} is reduced using the self-forward-body-bias technique [5]. Connecting resistor R_{BS} to the body terminal of transistors M_1 and M_2 causes a forward body-to-source biasing, subsequently lowering threshold voltage V_T of both transistors and ultimately reducing V_{DD}. Thus, the value of resistor R_{BS} should be designed as

$$R_{BS} = \frac{V_{DD} - V_{BS1} - V_{SB2}}{I_{S1}\left[e^{(V_{BS1}/\eta V_T)} - 1\right]} \tag{2}$$

where η is the ideality factor, I_{S1} is the reverse-bias leakage current of transistor M_1, V_{BS1} is the bulk–source p-n junction voltage of transistor M_1, and V_{SB2} is the bulk–source p-n junction voltage of transistor M_2. Additionally, the input impedance $Z_{\rm in}(j\omega)$ and the noise factor F of the submilliwatt LNA are given by [6]

$$Z_{\rm in}(j\omega) \approx \frac{R_F + j\omega L_1 \| r_o}{1 + (g_{m1} + g_{m2})(j\omega L_1 \| r_o)} \tag{3}$$

$$F \approx 1 + \frac{\gamma}{\alpha}\frac{1}{(g_{m1} + g_{m2})R_S} \tag{4}$$

where R_F is the self-feedback resistor, R_S is the source impedance, r_o is the effective small-signal output resistance of two parallel transistors M_1 and M_2, g_{m1} is the transconductance of transistor M_1, g_{m2} is the transconductance of transistor M_2, γ is the thermal noise coefficient of a transistor, and α is the ratio of g_m to zero-bias drain conductance. According to (3) and (4), transconductances g_{m1} and g_{m2} are chosen as a tradeoff between the noise figure (NF) and the input matching when the self-feedback resistor R_F is designed. The output of the LNA connects to the primary winding inductance of the trifilar transformer splitter L_1.

C. SOM

This work also attempts to further reduce the power consumption of the proposed receiver by using SOM architecture [7] in order to merge the ILO and the PD in Fig. 2 into one component with current reuse, as shown in Fig. 4. The ILO in the SOM has an active core, consisting of two transistors, i.e., M_3 and M_4, and a passive tank that comprises the secondary winding inductance L_2 and varactors $C_{\rm Var}$. This ILO achieves a tuning range of 2–2.8 GHz. As long as the locking range of the ILO is much larger than the frequency shift due to the process–voltage–temperature (PVT) variations in the free-running state, the ILO can be stably locked in the tuning bandwidth by a received co-frequency signal.

Primary and secondary winding inductances L_1 and L_2 form a balun to provide a differential injection signal to the ILO. As mentioned earlier, a lower $I_{\rm osc}$ implies a larger demodulation bandwidth. Thus, both M_3 and M_4 are biased in the subthreshold region, providing a sufficiently high g_m value with an ultralow $I_{\rm osc}$. Moreover, the V_T values of both M_3 and M_4 are lowered using the body-biasing network, which comprises resistor R_{BD} and capacitor C_G, subsequently allowing the ILO

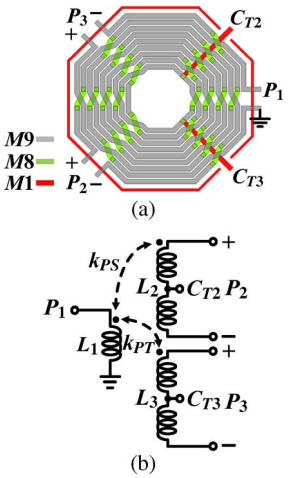

Fig. 5. Symmetrical trifilar transformer splitter. (a) Layout structure. (b) Equivalent circuit.

to operate at a low supply voltage of $V_{DD2} = V_{GS3} - V_T$. The Gilbert-cell switching stage comprises transistors $M_5 - M_8$, which are biased in the saturation region to increase conversion gain k_c. Thus, the minimum supply voltage V_{DD1} for the SOM is given by

$$V_{DD1} = V_{DD2} + V_{GS5} + V_{RL} - 2V_T - V_{\text{osc}} \tag{5}$$

where V_{GS5} is the gate–source voltage of transistor M_5, V_{RL} is the across voltage of resistor R_L, and V_{osc} is the oscillating voltage of the ILO. According to (5), the R_L value should be reasonably designed since it reduces the voltage headroom of the Gilbert-cell switching stage, subsequently lowering the linearity of the SOM. Additionally, primary and tertiary winding inductances L_1 and L_3 also act as a balun to perform differential injection in order to feed the Gilbert-cell switching stage with the LNA output signal.

D. Trifilar Transformer Splitter

To magnetically couple the LNA output signal to the SOM inputs, as shown in Fig. 2, a transformer splitter with three interlaced wires is adopted in this work. As depicted in Fig. 5(a), the center taps, i.e., C_{T2} and C_{T3}, which are in the secondary and tertiary windings, are used as a biasing path. Fig. 5(b) shows the equivalent circuit of the trifilar transformer splitter, where k_{PS} is the coefficient of the magnetic coupling between the primary and secondary windings, and k_{PT} is the coefficient of the magnetic coupling between the primary and tertiary windings. Generally, the values of both k_{PS} and k_{PT} are around 0.6–0.8 when the trifilar transformer splitter is implemented on a silicon substrate.

III. Circuit Design

The proposed receiver was designed and fabricated using a 90-nm CMOS 1P9M technology. In the submilliwatt LNA design, a g_m value of 14 mS was yielded by using M_1 with a gate width of 5×6 μm and M_2 with a gate width of 5×18 μm. Additionally, an input return loss of 14 dB, a voltage gain of 24 dB, and an NF of 2.4 dB in the 2.3- to 2.5-GHz band were achieved using a R_F value of 2.3 kΩ. Furthermore, a R_{BS} value

TABLE I
Device Information for the Proposed Circuit Design

Bias current	I_{LNA}			I_{SOM}		
Value	1.1 mA			2 mA		
Transistors	**M_1**	**M_2**		**M_{3-4}**	**M_{5-8}**	
W/L (μm/nm)	30/90	90/90		224/90	40/90	
Transformer	**Radius**	**Width**		**k_{PS}**	**k_{PT}**	
Value	190 μm	10 μm		0.76	0.76	
Passives	$R_{B,BD}$ [a]	R_{BS} [a]	R_F [a]	R_L [a]	$C_{G,B}$ [b]	C_{Var} [c]
Value	5 kΩ	7 kΩ	2.3 kΩ	0.8 kΩ	4 pF	.6–2 pF

[a] P+ poly resistor; [b] Metal-insulator-metal capacitor; [c] MOS varactor

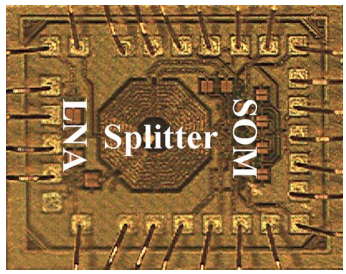

Fig. 6. Photograph of the implemented injection-locked GFSK receiver.

of 7 kΩ was determined to obtain a supply voltage of 0.8 V. In the SOM design, the g_m value of M_3 and M_4 was set to 20 mS, with a gate width of 4×56 μm; whereas the g_m value of $M_5 - M_8$ was set to 3 mS, with a gate width of 2×20 μm. With these settings, a voltage gain of 8 dB can be achieved for the SOM. In addition, the output resistor R_L with a resistance of 800 Ω was used to cause the Gilbert-cell switching stage to operate at saturation. The trifilar transformer splitter was formed mainly on the top metal layer of the CMOS process, with a thickness of 3.4 μm. The designed primary to secondary to tertiary turn ratio was 3: 3: 3; and the parameters of the trifilar transformer splitter, which were extracted from electromagnetic (EM) simulation at 2.4 GHz, were $k_{PS} \approx k_{PT} \approx 0.76$, $L_1 = 3.9$ nH and $L_2 = L_3 = 4$ nH. According to EM simulation results, the voltage coupling loss is 1.9 dB. More detailed device information is shown in Table I.

IV. Simulated and Experimental Results

In the simulation, the standard Bluetooth GFSK modulated signal is applied to the proposed injection-locked receiver. To meet the Bluetooth standard requirements of -70 dBm sensitivity and -20 dBm maximum signal strength at a 10^{-3} bit error rate (BER), the minimum locking range of the ILO is set at 4 MHz for the received Bluetooth signal with a data rate up to 2 Mb/s to ensure locking stability, whereas the maximum saturation power of the LNA is set at -15 dBm to prevent phase-to-frequency distortion of the ILO.

The proposed injection-locked GFSK was fabricated in a 90-nm RF CMOS 1P9M technology and then measured using a chip on board a 0.8-mm-thick FR4 substrate. Fig. 6 shows a photograph of the implemented receiver chip. The chip area is 0.56×0.76 mm^2. During the demodulation test, an external operational amplifier with a power consumption of 0.84 mW was used as an output buffer. The power consumption of the chip alone is 1.8 mW.

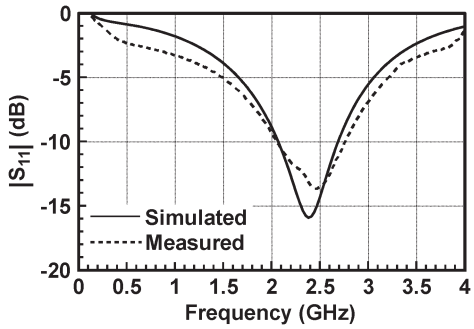

Fig. 7. Simulated and measured input return loss of the implemented injection-locked GFSK receiver.

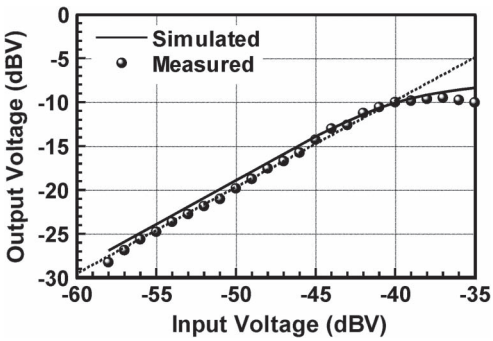

Fig. 8. Simulated and measured output versus the input voltage of the implemented injection-locked GFSK receiver.

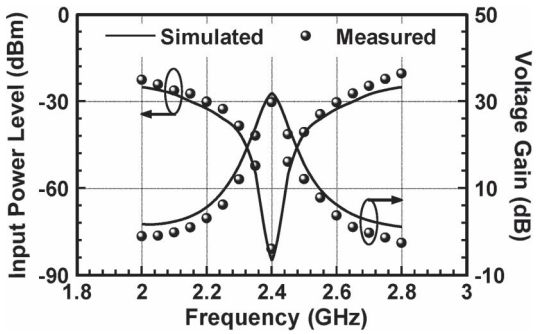

Fig. 9. Simulated and measured input power level and voltage gain in the boundary of the locking range.

As a continuous-wave test result, Fig. 7 shows the input return loss $|S_{11}|$ of the receiver. The measured $|S_{11}|$ is less than -10 dB over the 2- to 2.8-GHz band. Fig. 8 shows the linearity of the receiver. The input 1-dB gain compression point is -39 dBV (-27.2 dBm), mainly resulting from the saturation of the LNA. Fig. 9 shows the input power level and voltage gain of the receiver operating in the boundary of the locking range. Measurement results indicate that the receiver achieves a minimum lockable signal level of -84 dBm with a voltage gain of 30 dB. Fig. 10 shows the simulated and measured phase noises of the unlocked ILO at 2.4 GHz. The phase noise was measured using on-chip test buffers, achieving -114.6 dBc/Hz at an offset frequency of 1 MHz. The deviation of the simulated phase–noise curve from the measured one is primarily due to the noise from the power supply. Since the phase noise of the ILO is dominated by the injection signal, the degradation in the free-running phase noise hardly influences the performance of the proposed injection-locked receiver.

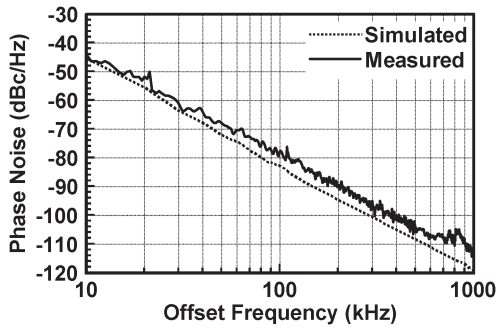

Fig. 10. Simulated and measured phase noises of the unlocked ILO.

TABLE II
COMPARISON OF THE LOCKING RANGE BETWEEN THIS WORK AND OTHER INJECTION-LOCKED RECEIVER DESIGNS

Reference	Frequency	P_{inj} for ω_{LR}/ω_o = 0.02	Power consumption
This work	2.4 GHz	-59 dBm	1.8 mW
[1]	60 GHz	-14 dBm *	41 mW
[8]	0.915 GHz	-41 dBm *	0.216 mW
[9]	0.3 GHz	-47 dBm *	0.12 mW

P_{inj}: injection power; *graphically estimated

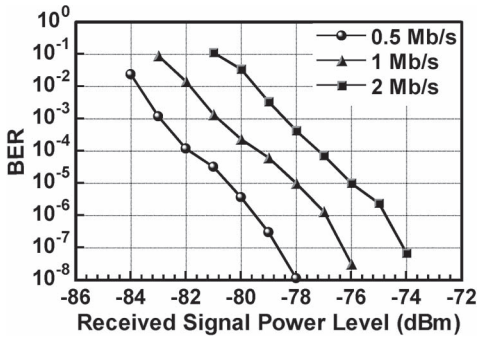

Fig. 11. Measured BER of the Bluetooth GFSK signals with different data rates.

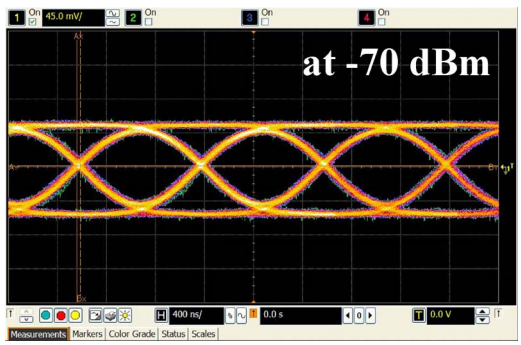

Fig. 12. Measured eye diagram of the Bluetooth GFSK signal at 1 Mb/s with a received signal level of -70 dBm.

Table II compares the locking range of this work with those of other injection-locked receiver designs [8], [9]. Based on the comparison, this work presents a minimum injection power level for a 0.02 of normalized $\omega_{\rm LR}/\omega_o$. Thus, the proposed receiver has a higher sensitivity than those of the compared injection-locked receivers. In the demodulation test, a Bluetooth GFSK signal with data rates of 0.5, 1, and 2 Mb/s were used, respectively. Fig. 11 plots the measured BER versus the received signal level for different data rates. The sensitivities

TABLE III
PERFORMANCE COMPARISON OF THIS WORK WITH OTHER 2.4-GHZ BLUETOOTH GFSK RECEIVER DESIGNS

Reference	Data Rate	Sensitivity for BER =10^{-3}	Power Consumption	CMOS Technology
This work	1 Mb/s	-81 dBm	1.8 mW [a]	90 nm
[10]	1 Mb/s	-91 dBm	25.2 mW [b]	65 nm
[11]	1 Mb/s	-92 dBm	27.9 mW [c]	130 nm
[12]	1 Mb/s	-82.5 dBm	9.12 mW [d]	180 nm

[a] exclude external operation amplifier
[b] include variable gain LNA, demodulator, synthesizer, IF amplifier, and analog to digital converter (ADC)
[c] include variable gain LNA, demodulator, synthesizer, IF amplifier, ADC, and power management circuits
[d] include variable gain LNA, demodulator, synthesizer, and IF amplifier

for a BER of 10^{-3} at data rates of 0.5, 1, and 2 Mb/s are -83.2, -81, and -78.4 dBm, respectively, thus meeting the Bluetooth sensitivity specification of -70 dBm. Additionally, the maximum signal strength for all data rates exceeds -20 dBm. Fig. 12 displays an eye diagram of the Bluetooth GFSK signal at 1 Mb/s with a received signal level of -70 dBm, revealing a clear eye opening with a low peak-to-peak jitter. Table III summarizes the performance merits of the proposed receiver and compares them with those of PLL-based designs for Bluetooth GFSK receivers [10]–[12]. That comparison reveals that, despite its moderate sensitivity, the proposed receiver consumes significantly less power than PLL-based designs do. Thus, the proposed receiver is more suitable for the SRW systems with strict low power consumption requirements.

V. CONCLUSION

This brief has presented a novel injection-locked GFSK receiver. Based on the current-reused RF circuitry combined with a trifilar transformer splitter and an ultralow-current SOM, the proposed receiver significantly improves in both sensitivity and power consumption. Measurement results demonstrate a superior demodulation of Bluetooth GFSK signals with an ultralow power consumption of 1.8 mW.

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