Enhancement of Frequency Synthesizer Operating Range Using a Novel Frequency-Offset Technique for LTE-A and CR Applications

Kang-Chun Peng, *Member, IEEE*, Chan-Hung Lee, Chung-Hung Chen, and Tzyy-Sheng Horng, *Senior Member, IEEE*

***Abstract*—This paper presents a novel frequency-offset technique to enhance operating range of frequency synthesizers for long-term evolution-advanced and cognitive-radio applications. Conventional wideband frequency synthesizers typically have complex architectures, such as multiple phase-locked loops (PLLs), multiple voltage-controlled oscillators, and multiple mixers, to increase operating range. These complex architectures have high cost and power consumption. In this study, the proposed technique substantially increases the operating range of the frequency synthesizer by using only a single PLL to simultaneously lock two mixing oscillators. The presented frequency synthesizer is implemented using 0.18-μm CMOS technology. Performance tests demonstrate that the frequency synthesizer achieves a very wide operating frequency range from 50 MHz to 4.8 GHz with a phase noise lower than -100 dBc/Hz at a frequency offset of 100 kHz. The period of stability for a switching frequency of 40 MHz is shorter than 40 μs.**

***Index Terms*—Cognitive radio (CR), long-term evolution-advanced (LTE-A), phase-locked loop (PLL), wideband frequency synthesizer, wideband voltage-controlled oscillator (VCO).**

I. Introduction

SMARTPHONE use has increased globally because of their many capabilities and their convenience for downloading and uploading information through diversified wireless systems. The rapid adoption of smartphones requires new technologies for maximizing usage of the fractional spectrum. The long-term evolution-advanced (LTE-A) system adopts a carrier aggregation technique to expand its bandwidth. The technique aggregates up to five 20-MHz-wide channels from inter-bands or intra-bands [1]. This adaptive carrier aggregation forms a logical 100-MHz-wide bandwidth. The IEEE 802.22 wireless regional area network (WRAN) uses the cognitive-radio (CR) technique to exploit white spaces in the TV spectrum [2]. However, both highly spectrum efficient wireless systems use widespread fractional spectrum. According to specifications, smartphones require an operating range from 50 MHz to 3.8 GHz for supporting both IEEE 802.22 and LTE-A systems [1], [2]. The operating range may be even wider as the CR technique is introduced to higher frequency bands. This wide operating range is a major challenge for the frequency synthesizers that provide local oscillators (LOs) for up-and down-conversion of modulated signals in RF transceivers [3]. The main bottleneck of this challenge is that a single voltage-controlled oscillator (VCO) in a traditional frequency synthesizer is incapable of oscillating from 50 MHz to 3.8 GHz with a fractional bandwidth close to 200%.

Several wideband frequency synthesizer architectures have been proposed to increase operating range. Fig. 1(a) shows how a wideband frequency synthesizer can be achieved by using multiple phase-locked loops (PLLs), each of which covers a specified band [3]–[10]. Additionally, the operating range can be expanded without increasing the number of PLLs by mixing PLL outputs to cover specified bands. The main disadvantage of this architecture is that using multiple PLLs increases both cost and power consumption. Fig. 1(b) shows a wideband frequency synthesizer that uses multiple VCOs in a PLL [11]–[13]. The PLL locks one VCO at a time to cover a specified band. Compared to architecture with multiple PLLs, this approach has lower cost and power consumption at the expense of system stability.

Fig. 1(c) presents a wideband frequency synthesizer that uses multiple band-selecting dividers and mixers [14]–[25]. This architecture requires only one PLL and VCO to synthesize a fundamental frequency. All other specified frequencies are synthesized by repeatedly dividing and mixing the fundamental frequency. Therefore, this wideband frequency synthesizer requires complex and precise frequency planning [15]. Additionally, it requires complex filter banks for removing spurious and image signals are created in complex signal mixing. The complex filter banks not only increase the cost of the frequency synthesizer, but they also complicate integration. Moreover, the above wideband frequency synthesizers only cover specified commercial bands. Increasingly complex circuitry is required as new bands are included in the system.

In this paper, a novel frequency-offset technique is proposed to expand the operating range of a frequency synthesizer. The proposed technique enables one PLL to lock and output the

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K.-C. Peng is with the Department of Computer and Communication Engineering, National Kaohsiung First University of Science and Technology, Kaohsiung City 811, Taiwan (e-mail: peterpkg@nkfust.edu.tw).

C.-H. Lee is with the Institute of Engineering Science and Technology, National Kaohsiung First University of Science and Technology, Kaohsiung City 811, Taiwan (e-mail: zoneaa_li@hotmail.com).

C.-H. Chen and T.-S. Horng are with the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung City 804, Taiwan (e-mail: genechen98@gmail.com; jason@ee.nsysu.edu.tw).

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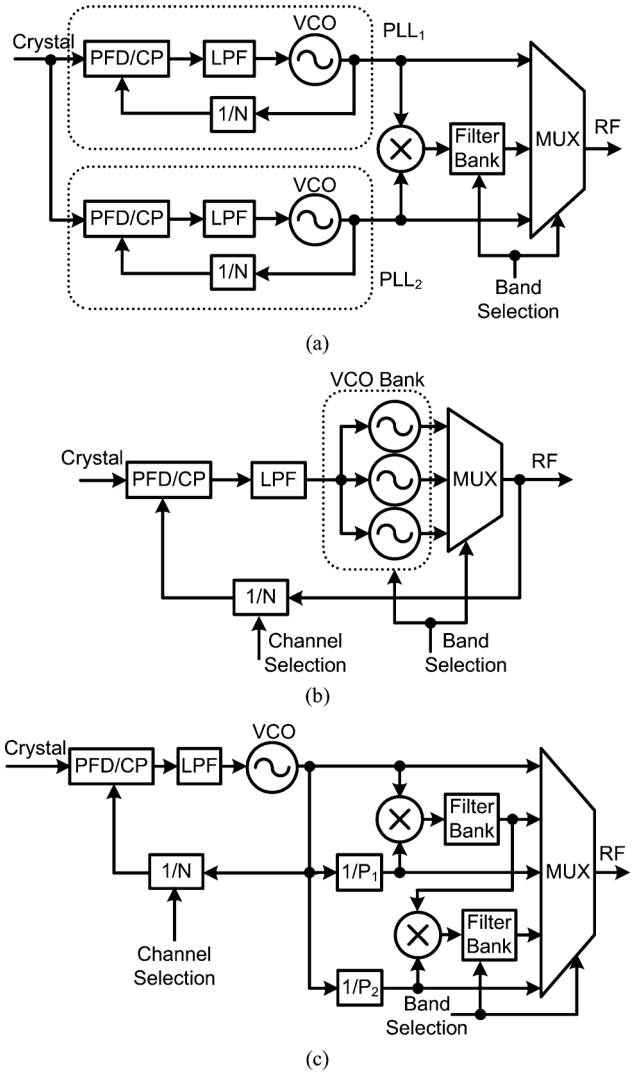

Fig. 1. Conventional wideband frequency synthesizer using: (a) multiple PLLs, (b) multiple VCOs, and (c) multiple band-selecting dividers and mixers.

mixing frequency of two oscillators, where one is permanently free running. Accordingly, a wideband CMOS frequency synthesizer design is presented to validate the effectiveness of the proposed technique. In contrast with the conventional wideband frequency synthesizers mentioned above, the presented synthesizer has a continuous ultra-wide tuning range and a relatively simple architecture.

II. Architecture and System Analysis

A. Architecture

Fig. 2 presents the proposed wideband frequency synthesizer that exploits a novel frequency-offset technique. In contrast with a conventional offset-PLL that uses two PLLs in a fractional-N synthesizer to reduce quantization noise and avoid frequency pulling [26], the proposed synthesizer resembles a conventional offset-PLL, except that its operating range is increased using a free-running VCO to up-convert or down-convert the frequency of the main VCO. The PLL then locks and outputs the converted frequency. The system architecture is simplified by using

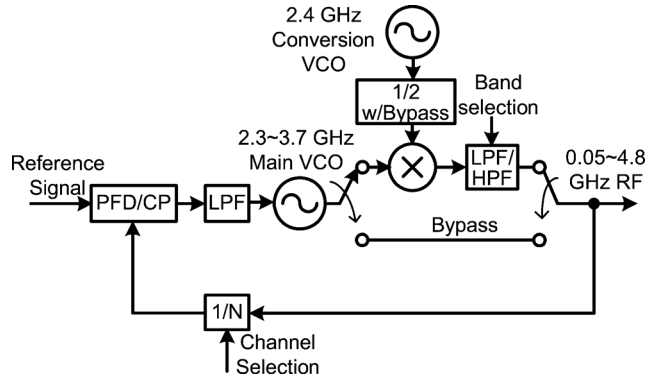

Fig. 2. 50-MHz–4.8-GHz wideband frequency synthesizer using the proposed frequency-offset technique.

a single wideband mixer for both up- and down-conversion. Accordingly, the synthesizer uses a fifth-order low-pass filter (LPF) and a fifth-order high-pass filter (HPF) as band-selecting filters. Either up- or down-conversion type can be determined by simply switching between the LPF and HPF. Since the cutoff frequencies of these filters are generally far away from the PLL bandwidth, the dynamics of the synthesizer would not be affected by the filters. This unique frequency-offset mechanism has a simpler architecture, but a larger operating bandwidth than conventional wideband frequency synthesizers. Furthermore, the operating band of the proposed frequency synthesizer is continuous. Hence, the complexity of the proposed architecture is independent of the spectral distribution of the system.

B. Stability Analysis

Fig. 3 shows a linear model to analyze the stability of the frequency synthesizer with the proposed frequency-offset technique in which a second-order loop filter is used. In the linear model, K_d denotes the combined gain of the phase-frequency detector (PFD) and charge pump (CP), and K_v denotes the sensitivity of the main VCO. The phases of the free-running conversion VCO and the reference signal are denoted by $\phi_{\mathrm{CVCO}}(s)$ and $\phi_{\mathrm{ref}}(s)$, respectively. The detected phase error is denoted by $\phi_e(s)$. N is the division ratio of the divider. $F(s)$ represents the transfer function of the loop filter and is shown as

$$F(s) = \frac{sRC_2 + 1}{s(sRC_1C_2 + C_1 + C_2)}. \tag{1}$$

The detected phase error can be derived as

$$\begin{aligned}\phi_e(s) &= \phi_{\mathrm{ref}}(s)H_e(s) + \phi_{\mathrm{CVCO}}(s)\frac{H_e(s)}{N} \\ &= \phi_{e,\mathrm{ref}}(s) + \phi_{e,\mathrm{CVCO}}(s)\end{aligned} \tag{2}$$

where

$$\phi_{e,\mathrm{ref}}(s) = \phi_{\mathrm{ref}}(s)H_e(s) \tag{3}$$

$$\phi_{e,\mathrm{CVCO}}(s) = \phi_{\mathrm{CVOC}}(s)\frac{H_e(s)}{N} \tag{4}$$

$$\begin{aligned}H_e(s) &= \frac{Ns}{Ns + K_vK_dF(s)} \\ &= \frac{Ns^2(sRC_1C_2 + C_1 + C_2)}{Ns^2(sRC_1C_2 + C_1 + C_2) + (sRC_2 + 1)K_vK_d}.\end{aligned} \tag{5}$$

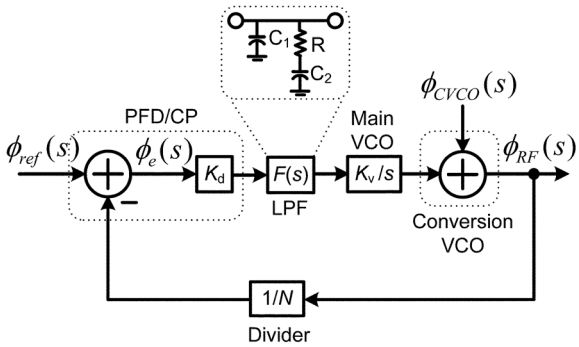

Fig. 3. Linear model of the wideband frequency synthesizer with the proposed frequency-offset technique.

For a step variation in the phase of the reference signal and of the conversion VCO, (3) and (4) can be respectively written as

$$\phi_{e,\mathrm{ref}}(s) = \mathfrak{L}\left\{\Delta\phi\, u(t)\right\} H_e(s) = \frac{\Delta\phi H_e(s)}{s} \tag{6}$$

$$\phi_{e,\mathrm{CVCO}}(s) = \mathfrak{L}\left\{\Delta\phi\, u(t)\right\} \frac{H_e(s)}{N} = \frac{\Delta\phi H_e(s)}{Ns} \tag{7}$$

where $\Delta\phi$ represents the phase step, $u(t)$ represents a step function, and $\mathfrak{L}$ denotes the Laplace transform. Based on the final value theory, the detected phase errors $\phi_{e,\mathrm{ref}}$ and $\phi_{e,\mathrm{CVCO}}$ in the time domain as $t \to \infty$ can be, respectively, found as

$$\theta_{e,\mathrm{ref}}(t\to\infty) = \lim_{s\to 0} s\,\phi_{e,\mathrm{ref}}(s) = \lim_{s\to 0} \Delta\phi H_e(s) = 0 \tag{8}$$

$$\theta_{e,\mathrm{CVCO}}(t\to\infty) = \lim_{s\to 0} s\,\phi_{e,\mathrm{CVCO}}(s) = \lim_{s\to 0} \frac{\Delta\phi H_e(s)}{N} = 0. \tag{9}$$

For a step variation in the frequency of the reference signal and of the conversion VCO, (3) and (4) can, respectively, lead to

$$\phi_{e,\mathrm{ref}}(s) = \mathfrak{L}\left\{\int \Delta\omega\, u(t)dt\right\} H_e(s) = \frac{\Delta\omega H_e(s)}{s^2} \tag{10}$$

$$\phi_{e,\mathrm{CVCO}}(s) = \mathfrak{L}\left\{\int \Delta\omega\, u(t)dt\right\} \frac{H_e(s)}{N} = \frac{\Delta\omega H_e(s)}{Ns^2} \tag{11}$$

where $\Delta\omega$ represents the frequency step. The detected phase errors $\phi_{e,\mathrm{ref}}$ and $\phi_{e,\mathrm{CVCO}}$ in the time domain as $t \to \infty$ can be, respectively, found as

$$\begin{aligned}\phi_{e,\mathrm{ref}}(t\to\infty) &= \lim_{s\to 0} s\,\phi_{e,\mathrm{ref}}(s)\\ &= \lim_{s\to 0} \frac{\Delta\omega H_e(s)}{s}\\ &= 0\end{aligned} \tag{12}$$

$$\begin{aligned}\theta_{e,\mathrm{CVCO}}(t\to\infty) &= \lim_{s\to 0} s\,\phi_{e,\mathrm{CVCO}}(s)\\ &= \lim_{s\to 0} \frac{\Delta\omega H_e(s)}{Ns}\\ &= 0.\end{aligned} \tag{13}$$

Equation (8), (9), (12), and (13) reveal that the proposed wideband frequency synthesizer can yield a locked state regardless of variations in phase and frequency steps.

When the frequency drift of the reference signal and of the conversion VCO occurs, (3) and (4) can, respectively, become

$$\begin{aligned}\phi_{e,\mathrm{ref}}(s) &= \mathfrak{L}\left\{\int \Delta\omega'_{\mathrm{ref}}\, t\, dt\right\} H_e(s)\\ &= \frac{\Delta\omega'_{\mathrm{ref}} H_e(s)}{s^3}\end{aligned} \tag{14}$$

$$\begin{aligned}\phi_{e,\mathrm{CVCO}}(s) &= \mathfrak{L}\left\{\int \Delta\omega'_{\mathrm{CVCO}}\, t\, dt\right\} \frac{H_e(s)}{N}\\ &= \frac{\Delta\omega'_{\mathrm{CVCO}} H_e(s)}{Ns^3}\end{aligned} \tag{15}$$

where $\Delta\omega'_{\mathrm{ref}}$ and $\Delta\omega'_{\mathrm{CVCO}}$ represent the rates of frequency drift of the reference signal and the conversion VCO, respectively. The detected phase errors $\phi_{e,\mathrm{ref}}$ and $\phi_{e,\mathrm{CVCO}}$ in the time domain as $t \to \infty$ can be derived as

$$\begin{aligned}\theta_{e,\mathrm{ref}}(t\to\infty) &= \lim_{s\to 0} s\,\phi_{e,\mathrm{ref}}(s)\\ &= \lim_{s\to 0} \frac{\Delta\omega'_{\mathrm{ref}} H_e(s)}{s^2}\\ &= \frac{\Delta\omega'_{\mathrm{ref}}}{(2\pi f_n)^2}\end{aligned} \tag{16}$$

$$\begin{aligned}\theta_{e,\mathrm{CVCO}}(t\to\infty) &= \lim_{s\to 0} s\,\phi_{e,\mathrm{CVCO}}(s)\\ &= \lim_{s\to 0} \frac{\Delta\omega'_{\mathrm{CVCO}} H_e(s)}{Ns^2}\\ &= \frac{\Delta\omega'_{\mathrm{CVCO}}}{N(2\pi f_n)^2}\end{aligned} \tag{17}$$

where

$$f_n = \frac{1}{2\pi}\sqrt{\frac{K_v K_d}{N(C_1+C_2)}} \tag{18}$$

is the PLL bandwidth of the proposed frequency synthesizer. Since both the reference signal and the conversion VCO exhibit frequency drift, the overall detected phased error in the time domain can be found as

$$\begin{aligned}\theta_e(t\to\infty) &= \theta_{e,\mathrm{ref}}(t\to\infty) + \theta_{e,\mathrm{CVCO}}(t\to\infty)\\ &= \frac{\Delta\omega'_{\mathrm{ref}}}{(2\pi f_n)^2} + \frac{\Delta\omega'_{\mathrm{CVCO}}}{N(2\pi f_n)^2}.\end{aligned} \tag{19}$$

Since the maximum detectable phase error of a PFD is 2π, (19) can be rewritten as

$$\theta_e(t\to\infty) = \frac{\Delta\omega'_{\mathrm{ref}}}{(2\pi f_n)^2} + \frac{\Delta\omega'_{\mathrm{CVCO}}}{N(2\pi f_n)^2} < 2\pi. \tag{20}$$

The condition for convergence toward a locked state can then be found as

$$N\Delta\omega'_{\mathrm{ref}} + \Delta\omega'_{\mathrm{CVCO}} < N(2\pi)^3 f_n^2. \tag{21}$$

Under the condition described by (21), the locking process of the proposed wideband frequency synthesizer converges toward a locked state regardless of the variation of the reference signal

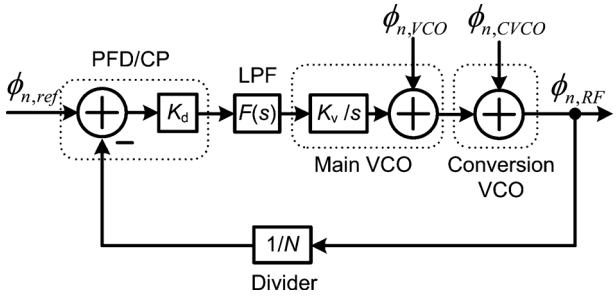

Fig. 4. Phase-noise model of the proposed wideband frequency synthesizer.

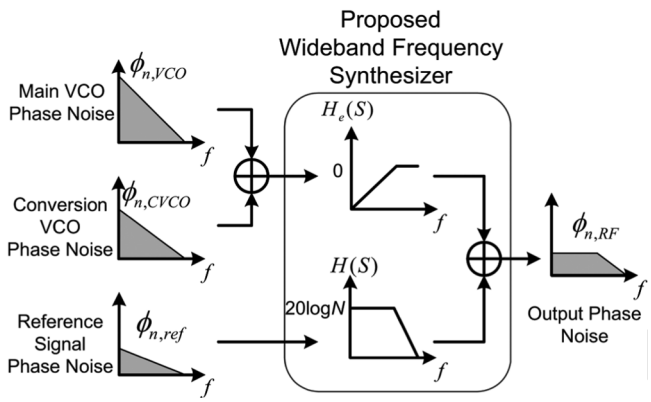

Fig. 5. Phase-noise suppression of the proposed wideband frequency synthesizer.

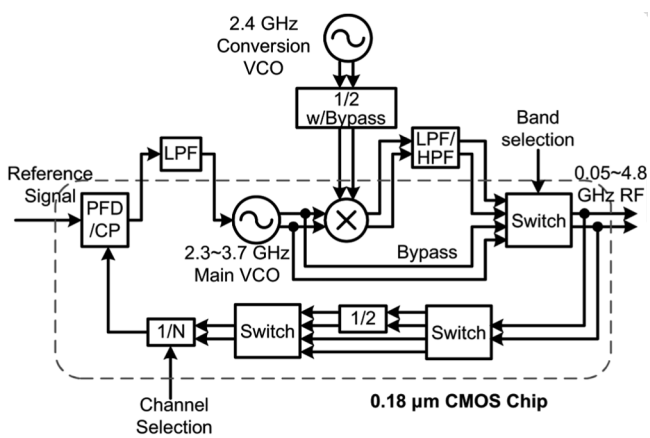

Fig. 6. Implementation of the proposed 50-MHz–4.8-GHz wideband frequency synthesizer.

and of the conversion VCO. Since (18)–(21) reveal that the characteristics of the conversion VCO do not affect the PLL bandwidth, the proposed synthesizer takes the same stable time regardless of the drift of the conversion VCO.

Theoretically, the phase margin and the gain margin of the open-loop gain determine the stability of a PLL-based frequency synthesizer in a locked state. With reference to Fig. 3, the open-loop gain of the proposed wideband frequency synthesizer is derived as

$$G(s) = \frac{K_v K_d F(s)}{Ns} = \frac{K_v K_d (sRC_2 + 1)}{Ns^2 (sRC_1 C_2 + C_1 + C_2)}. \quad (22)$$

TABLE I
FREQUENCY PLANNING OF THE PROPOSED 50-MHz–4.8-GHz WIDEBAND FREQUENCY SYNTHESIZER

Synthesis Frequency	Frequency Offset	External Conversion VCO	External Divid-by-2 Divider
50 MHz - 1.2 GHz	Down-conversion	Enable	Bypass
1.2 - 2.4 GHz	Down-conversion	Enable	Enable
2.4 - 3.6 GHz	Bypass	Disable	Disable
3.6 - 4.8 GHz	Up-conversion	Enable	Enable

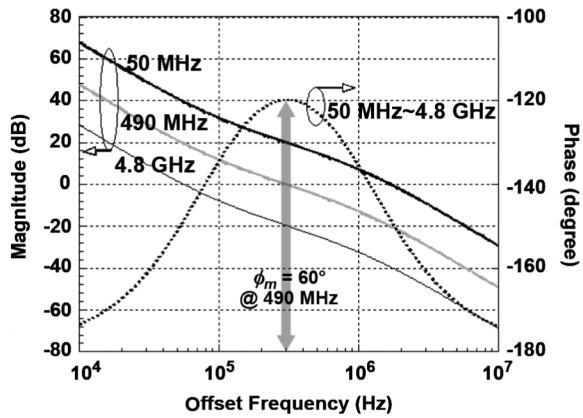

Fig. 7. Bode plot of the proposed wideband frequency synthesizer.

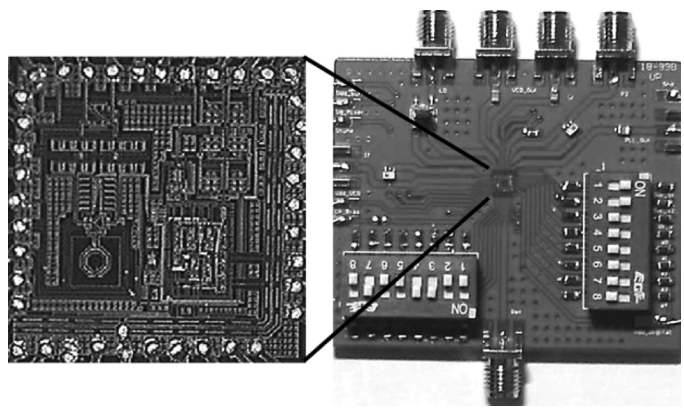

Fig. 8. Implemented CMOS chip of the 50-MHz–4.8-GHz wideband frequency synthesizer and test board.

Equation (22) indicates that the open-loop gain of the synthesizer is independent of the characteristics of the conversion VCO. Accordingly, the free running of the conversion VCO does not affect the stability of the proposed wideband synthesizer in a locked state.

C. Phase-Noise Analysis

The in-band phase noise of the synthesizer should be minimized since the LTE-A and IEEE 802.22 systems apply orthogonal frequency-division multiplexing (OFDM) technique to provide high spectral efficiency[27]. Fig. 4 presents the phase noise model that is used to analyze the suppression of the phase noise in the proposed frequency synthesizer. The phase noise from the main VCO, from the conversion VCO and from the reference signal, is denoted by $\phi_{n,\mathrm{VCO}}$, $\phi_{n,\mathrm{CVCO}}$, and $\phi_{n,\mathrm{ref}}$,

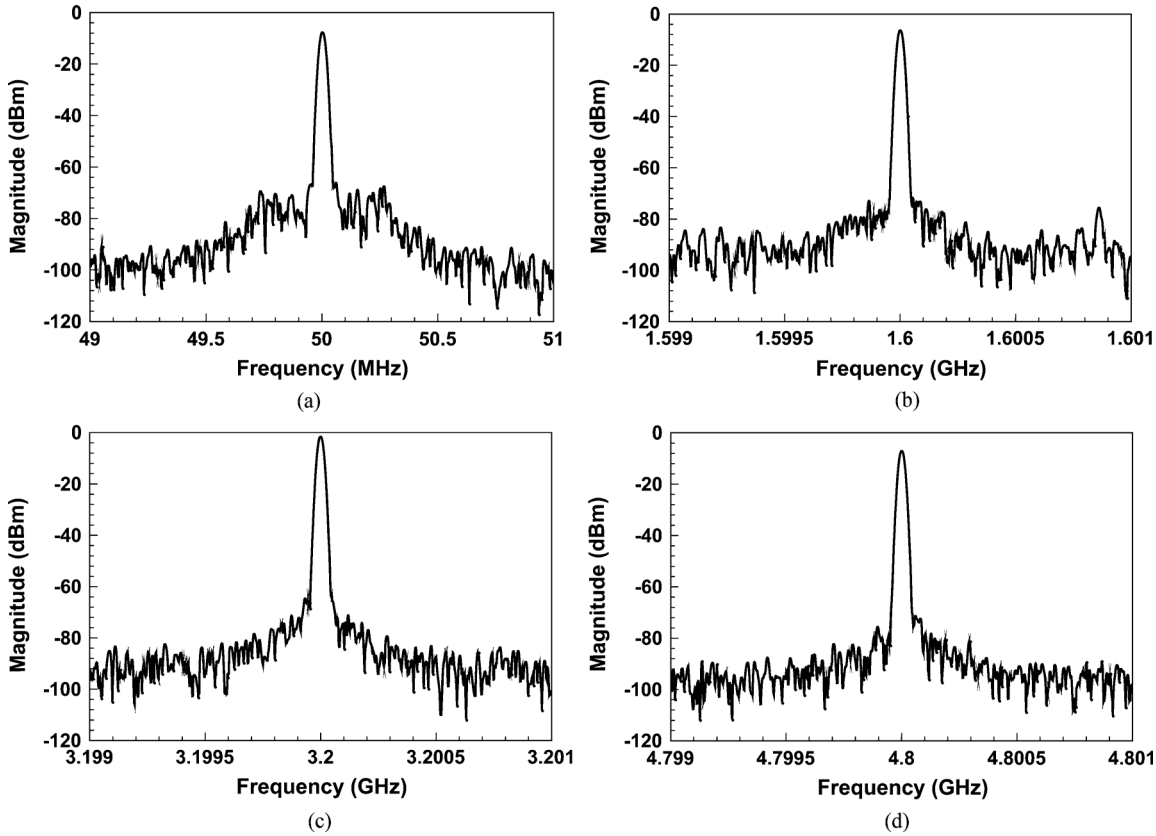

Fig. 9. Measured output spectra of the proposed frequency synthesizer at: (a) 50 MHz, (b) 1.6 GHz, (c) 3.2 GHz, and (d) 4.8 GHz.

respectively. The output phase noise of the proposed wideband frequency synthesizer can be derived as

$$\phi_{n,\mathrm{RF}}(s) = \phi_{n,\mathrm{ref}} H(s) + \left(\phi_{n,\mathrm{VCO}} + \phi_{n,\mathrm{CVCO}}\right) H_e(s) \quad (23)$$

where

$$H(s) = \frac{NK_vK_dF(s)}{Ns + K_vK_dF(s)} = \frac{NK_vK_d(sRC_2+1)}{Ns^2(sRC_1C_2 + C_1 + C_2) + (sRC_2+1)K_vK_d}. \quad (24)$$

Based on (5), (23), and (24), the suppression of the phase noise of the synthesizer can be depicted as shown in Fig. 5. The figure shows that the synthesizer can suppress the total phase noise of the main VCO and the conversion VCO inside the PLL bandwidth. These analytical results confirm that the synthesizer accurately tunes the main VCO to track the frequency and phase of the mixing signal and effectively suppresses the phase noise of the mixing signal.

III. System Design

To verify the proposed frequency-offset technique that can effectively expand the operating range, a wideband frequency synthesizer, shown in Fig. 6, is designed and implemented using TSMC 0.18-μm CMOS technology. For a prototype test, all the components, except for the free-running conversion VCO, the subsequent divide-by-2 divider with a bypass switch, and the band-selecting filters, are implemented in a CMOS chip.

A. Frequency Planning

The synthesizer is designed to operate at 50 MHz–4.8 GHz to maximize its potential for use in wireless applications. That is, the operation band includes not only the LTE-A and IEEE 802.22 frequency bands, but also other bands that have potential for use in future wireless applications such as CR. To achieve this wide operating band, the main VCO is designed to operate at 2.3–3.7 GHz. The free-running conversion VCO is designed to operate at a nominal frequency of 2.4 GHz. With these specifications, the 50-MHz–4.8-GHz operating band can be divided into the four sub-bands that are presented in Table I. The first sub-band at 50 MHz–1.2 GHz is achieved by down-converting the frequency of the main VCO using a 2.4-GHz free-running signal. As the external divide-by-2 divider is enabled, the synthesizer operates at 1.2–2.4 GHz in the down-conversion mode. In the up-conversion mode, a 3.6–4.8 GHz carrier can be synthesized using a 1.2-GHz free-running signal. Finally, the 2.4–3.6-GHz sub-band can be achieved simply by bypassing the frequency-offset mechanism.

B. Circuit Design

The key design considerations of the main VCO are its operating bandwidth and phase noise. Based on the above frequency related considerations, the main VCO requires a fractional bandwidth of 47% to cover 2.3–3.7 GHz. Generally, complementary

cross-coupled VCOs exhibit a better balance between low phase noise and wide operating bandwidth than nMOS and pMOS cross-coupled VCOs [28]. Therefore, the main VCO is designed with the complementary cross-coupled architecture. The wideband design considerations for the VCO tank demand the use of body-biased MOSFETs as varactors to provide a larger variation in capacitance than the use of conventional varactors. Hence, the operating bandwidth of the main VCO is substantially increased.

The phase-noise performance of the main VCO is optimized by applying impedance locus design methodology [29]. Current flow into the active circuit of the main VCO can be presented as

$$i = A\cos(\omega t + \phi) \tag{25}$$

where A and ω represent the magnitude and frequency of the current, respectively. The impedance locus $Z(A)$ of the active network and the impedance locus $Z(\omega)$ of the tank network can then be determined and depicted in a complex impedance plane. When these two loci cross each other at a particular frequency, an included angle is obtained. If the included angle at the intersection is between 0°–180°, the oscillation frequency of the VCO is the same as that at the intersection. However, if the included angle is 180°–360°, no oscillation occurs. Studies in [29] have shown that the phase-noise performance of the VCO is optimal when the included angle is 90°.

The proposed synthesizer in Fig. 6 reveals that the frequency-offset circuit, including a mixer and a switch, should have a wide operating range of 50 MHz–4.8 GHz. The wideband mixer design achieves this goal using a double-balanced passive switching architecture [30]. This passive mixer has a wider bandwidth and a greater linearity than the active Gilbert-cell mixer. However, since the conversion loss in the wideband passive mixer is considerable, the insertion loss of the wideband switch behind the mixer should be minimized to maintain an acceptable PLL output power. In the design, the wideband switch adopts the series-type single-pole double-throw (SPDT) architecture to achieve lower insertion loss and higher linearity than the series-shunt-type SPDT switch [31]. Another component of the proposed wideband synthesizer that must operate at 50 MHz–4.8 GHz is the programmable divider in the PLL feedback loop. The designed circuit of the divider is simplified by prescaling the synthesized frequency by a factor of 2, reducing the operating frequency range of the programmable divider to 50 MHz–2.4 GHz.

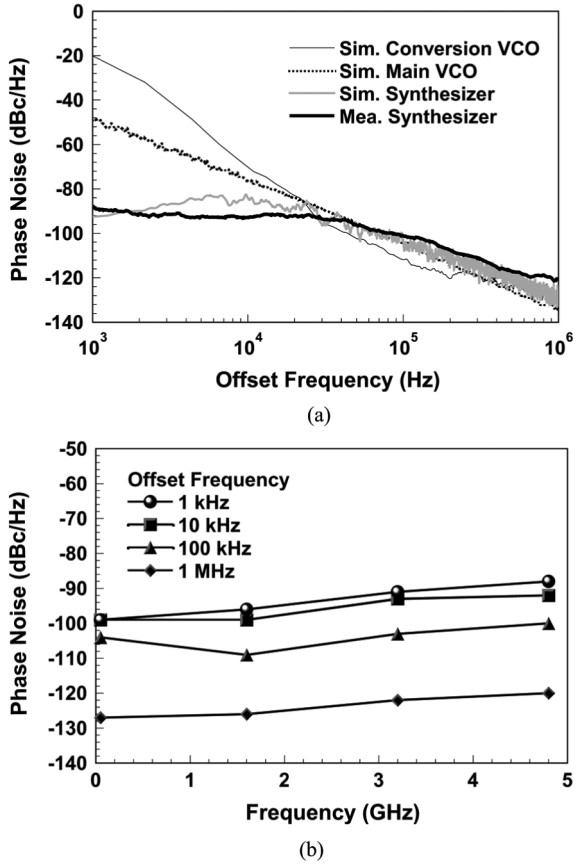

Fig. 10. Measured phase-noise performance of the proposed frequency synthesizer at: (a) 4.8 GHz with comparison of simulation results and (b) over the operating frequency range of 50 MHz–4.8 GHz.

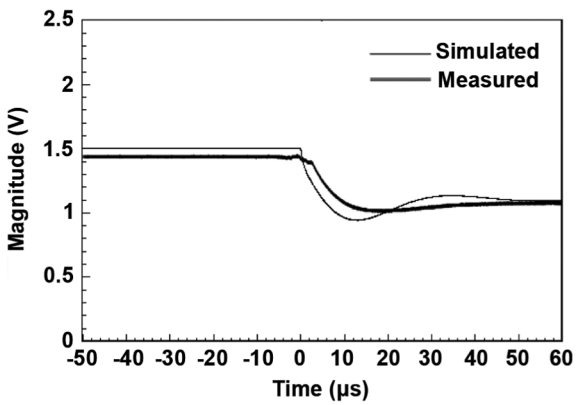

Fig. 11. Simulated and measured stable time of the proposed frequency synthesizer with switching frequency from 3.64 to 3.6 GHz.

C. System Design

In the system design, the stability of the proposed synthesizer is an important issue. Fig. 7 presents a bode plot of the proposed 50 MHz–4.8 GHz wideband frequency synthesizer, based on (22). It can be found that the magnitude of the open-loop gain has a considerable variation, which consequently results in a significant variation in phase margin ϕ_m. To ensure that the wideband frequency synthesizer is stable over the wide operating range, the loop filter must be designed with a center frequency of the operating band. Since the frequency information of a bode plot is presented in log scale, the center frequency f_c can be found with

$$10\log f_c = \frac{10\log f_{\max} + 10\log f_{\min}}{2} \tag{26}$$

where $f_{\max}$ and $f_{\min}$ denotes the maximum and minimum operating frequency of the frequency synthesizer. Based on (26), f_c can be re-derived as

$$f_c = \sqrt{f_{\max} f_{\min}} = \sqrt{4.8\,\text{GHz} \times 50\,\text{MHz}} \cong 490\ \text{MHz}. \tag{27}$$

TABLE II
COMPARISON OF RECENT WIDEBAND FREQUENCY SYNTHESIZERS

Reference	This work	[12] 09'RFIC	[14] 11'TMTT	[19] 10'JSSC	[17] 11'TVLSI	[4] 09'MWCL	[5] 07'TMTT
Operating frequency	50 MHz - 4.8 GHz	100 MHz - 5 GHz	54 - 862 MHz	0.8 - 1 GHz 1.6 - 2 GHz 2.4 - 3 GHz 4.8 - 6 GHz	3 - 10 GHz	3.4 - 9.2 GHz	3.1 - 10.6 GHz
Ratio of max-to-min operating frequency	96	50	16	7.5	3.3	2.7	3.4
Fractional bandwidth	196 %	192 %	176 %	22 % / band	108 %	92 %	109 %
Number of PLLs	1	1	1	1	1	2	3
Number of VCOs	2*	2	1	1	1	2	6
Number of mixers	1	0	0	1	3	6	1
Number of band-selecting dividers	0	6	4	3	5	2	0
Max operating frequency of VCOs	3.6 GHz	10 GHz	1.8 GHz	4 GHz	8.448 GHz	10.3 GHz	7.95 GHz
Max operating frequency of dividers	4.8 GHz	10 GHz	1.8 GHz	6 GHz	8.448 GHz	10.3 GHz	7.95 GHz
Reference frequency	10 MHz / 20 MHz	N/A	19.2 MHz	20 MHz	264 MHz	66 MHz	528 MHz
Phase noise at max operating frequency	-100 dBc/Hz @100kHz	-83 dBc/Hz @100kHz	-100 dBc/Hz @100kHz	-92 dBc/Hz @100kHz	-88 dBc/Hz @100kHz	-100 dBc/Hz @100kHz	-78 dBc/Hz @100kHz
Power dissipation	94 mW	51.1 mW	82.8 mW	88.2 mW	117 mW	55 mW	39 mW
Technology	0.18 μm CMOS	45 nm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	90 nm CMOS	0.13 μm CMOS

*Including an external free-running conversion VCO.

The wideband frequency synthesizer is then designed to have a 100-kHz PLL bandwidth and a 60° phase margin with an output frequency of 490 MHz. Under these conditions, Fig. 7 shows that the wideband frequency synthesizer has a phase margin ϕ_m of $30^\circ \sim 60^\circ$ over the wide operating range of 50 MHz $\sim$ 4.8 GHz. These results reveal that proposed wideband frequency synthesizer is stable.

IV. EXPERIMENTAL RESULTS

Fig. 8 shows the implemented test board of the 50-MHz–4.8-GHz wideband frequency synthesizer. The main circuit of the wideband synthesizer is fabricated using TSMC 0.18-μm CMOS technology and occupies an area of about 1.38×1.38 mm^2 of which approximately 50% is occupied by the main VCO and 50% is occupied by the PLL, mixer, and switch. The conversion VCO of this work is a Mini-Circuits product with a model number of ROS-3050-819+. The reference frequency is set as 10 and 20 MHz for a synthesized frequency range of 50–100 MHz and 100 MHz–4.8 GHz, respectively.

The measured frequency drift rates $\Delta\omega'_{\rm ref}$ and $\Delta\omega'_{\rm CVCO}$ are lower than 1 rad Hz/s and 20.1 rad MHz/s, respectively. Since $\Delta\omega'_{\rm CVCO}$ is much higher than $N\Delta\omega'_{\rm ref}$, (21) can then be rewritten as

$$N\Delta\omega'_{\rm ref} + \Delta\omega'_{\rm CVCO} \approx \Delta\omega'_{\rm CVCO} < N(2\pi)^3 f_n^2. \quad (28)$$

The maximum acceptable frequency drift rate of the free-running conversion VCO in this system is determined as

$$\Delta\omega'_{CVCO\_\max} = N_{\min}(2\pi)^3 f_n^2 = 12.4\,(\text{rad THz/s}) \quad (29)$$

where $N_{\min} = 5$ is the minimum division ratio. Since the measured $\Delta\omega'_{\rm CVCO}$ is much lower than $\Delta\omega'_{\rm CVCO\_max}$, the locking process of the implemented wideband frequency synthesizer certainly converges toward a locked state.

Fig. 9(a)–(d) shows the measured output spectrum of the implemented wideband frequency synthesizer at 50 MHz, 1.6 GHz, 3.2 GHz, and 4.8 GHz, respectively. These four spectra show that the proposed frequency synthesizer works flawlessly at the four sub-bands that are planned in Table I. Notably, the synthesized signal at 3.2 GHz has a 6 dB higher power than the others because it falls in the 2.4–3.6-GHz sub-band with a bypass of the wideband passive mixer and thus can save the 6-dB conversion loss.

Fig. 10(a) and (b) shows the measured phase-noise performance of the proposed frequency synthesizer at the highest operating frequency of 4.8 GHz and over the entire operating band of 50 MHz to 4.8 GHz, respectively. The measured phase noise agrees quite well with the simulation results, as can be seen in Fig. 10(a). The measurement results at 4.8 GHz reveal that the proposed frequency synthesizer effectively suppresses the combined phase noise of the main VCO and the conversion VCO

within the PLL bandwidth of about 40 kHz. Moreover, the measured phase noises shown in Fig. 10(b) slightly degrade as the frequency increases. Basically, the phase noises at the low offset frequencies that fall within the PLL bandwidth are mainly contributed from the reference source, tending to increase with the synthesized frequency because of the rise of the division ratio of the divider. In contrast, the phase noises at the high offset frequencies primarily originate from the main VCO, tending also to increase with the synthesized frequency because of the degradation of the quality factor of the tank.

Fig. 11 shows the simulated and measured stable time of the implemented wideband frequency synthesizer for frequency switching from 3.64 to 3.6 GHz. The measured stable time agrees well with the simulated results. The implemented synthesizer takes about 40 μs to stabilize for a switching frequency of 40 MHz.

Table II shows the comparison of recent wideband frequency synthesizers. The proposed architecture achieves the largest ratio of maximum to minimum operating frequency and the widest fractional bandwidth, while it eliminates the need of using a bunch of mixers and of band-selecting dividers. Additionally, the maximum operating frequencies of VCOs and of dividers are much lower than those of the prior art [12]. Comparing with the prior arts [14], [17], [19], although this work has an additional conversion VCO, this work achieves a much higher ratio of maximum to minimum operating frequency. Besides, the operating bandwidth of this work is nearly six times the one of the prior art [14]. In contrast to the four discontinuously operating bands of the prior art [19], the operating frequency band of this work is continuous. Although the conversion VCO is external, the synthesizer's in-band phase-noise performance, which markedly affects the processing of OFDM signals, would not be degraded by using an on-chip conversion VCO instead. This is because the PLL error transfer function $H_e(s)$ that appears in (5) can effectively suppress the phase noise of the conversion VCO within the PLL bandwidth, as depicted in Fig. 5 and witnessed by Fig. 10(a). Therefore, even if the conversion VCO has a worse phase noise than predicted in Fig. 10(a), the proposed frequency synthesizer can maintain similar phase-noise performance.

V. Conclusion

This paper presented a novel wideband frequency synthesizer based on a unique frequency-offset technique for LTE-A and CR applications. The proposed wideband frequency synthesizer is realized using TSMC 0.18-μm CMOS technology. The wide 50-MHz–4.8-GHz operating range of the synthesizer covers not only the latest LTE-A and IEEE 802.22 frequency bands, but also other potential frequency bands that may be released in the future. The measured phase noise is lower than -100 dBc/Hz at an offset frequency of 100 kHz over the entire operating band width. The measured stable time is shorter than 40 μs for a frequency switching of 40 MHz.

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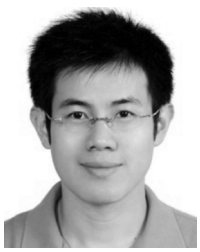

Kang-Chun Peng (S'00–M'05) was born in Taipei, Taiwan, on February 18, 1976. He received the B.S.E.E., M.S.E.E., and Ph.D. degrees from the National Sun Yat-Sen University, Kaohsiung, Taiwan, in 1998, 2000, and 2005, respectively.

He is currently an Assistant Professor with the Department of Computer and Communication Engineering, National Kaohsiung First University of Science and Technology, Kaohsiung, Taiwan. His current research interests are in the area of delta–sigma modulation techniques, ultra-low power VCOs, wideband frequency synthesizers, modulated frequency synthesizers, and coherent demodulators.

Chan-Hung Lee was born in Kaohsiung, Taiwan, on June 8, 1977. He received the B.S.E.E. degree from the National Kaohsiung University of Applied Sciences, Kaohsiung, Taiwan, in 2004, the M.S.E.E. degree from National Cheng Kung University, Tainan, Taiwan, in 2007, and is currently working toward the Ph.D. degree at the Institute of Engineering Science and Technology, National Kaohsiung First University of Science and Technology, Kaohsiung, Taiwan.

His research interests include ultra-low-noise frequency synthesizers, PLLs, OFDM receivers, and coherent demodulators.

Chung-Hung Chen was born in Kaohsiung, Taiwan, on December 26, 1976. He received the B.S.E.E. degree from National Cheng-Kung University, Tainan, Taiwan, in 2002, the M.S.E.E. degree from National Taiwan University, Taipei, Taiwan, in 2005, and is currently working toward the Ph.D. degree in electrical engineering at National Sun Yat-Sen University, Kaohsiung City, Taiwan. His doctoral research concerns low-power and wide-bandwidth frequency synthesizers.

Tzyy-Sheng Horng (S'88–M'92–SM'05) was born in Taichung, Taiwan, on December 7, 1963. He received the B.S.E.E. degree from National Taiwan University, Taipei, Taiwan, in 1985, and the M.S.E.E. and Ph.D. degrees from the University of California at Los Angeles (UCLA), in 1990 and 1992, respectively.

Since August 1992, he has been with the Department of Electrical Engineering, National Sun Yat-Sen University, Kaohsiung City, Taiwan, where he was the Director of the Telecommunication Research and Development Center (2003–2008), Director of the Institute of Communications Engineering (2004–2007), and where he is currently a Distinguished Professor. He has authored or coauthored over 200 technical publications published in refereed journals and conferences proceedings, mostly in IEEE publications. He holds over ten patents. His research interests include RF and microwave integrated circuits (ICs) and components, RF signal integrity for wireless system-in-package, digitally assisted RF technologies, and green radios for cognitive sensors and Doppler radars.

Dr. Horng has served on several Technical Program Committees of international conferences including the International Association of Science and Technology for Development (IASTED) International Conference on Wireless and Optical Communications, the IEEE Region 10 International Technical Conference, the IEEE International Workshop on Electrical Design of Advanced Packaging and Systems (EDAPS), the Asia–Pacific Microwave Conference (APMC), the IEEE Radio and Wireless Symposium (RWS), and the Electronic Components and Technology Conference (ECTC). He has also served on the Project Review Board of the Programs of Communications Engineering and Microelectronics Engineering of the National Science Council, Taiwan. He is the founder chair of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Tainan Chapter. He is currently an associate editor for the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES. He is a member of the IEEE MTT-S Technical Committee MTT-10 and MTT-20. He was the recipient of the 1996 Young Scientist Award presented by the International Union of Radio Science, the 1998 Industry–Education Cooperation Award presented by the Ministry of Education, Taiwan, and the 2010 Distinguished Electrical Engineer Award presented by the Chinese Institute of Electrical Engineering, Kaohsiung Branch, Taiwan. Recently, he was the recipient of the 2011 Advanced Semiconductor Engineering (ASE) Inc. Chair Professorship and the 2012 Outstanding Research Award of National Sun Yat-Sen University.