Ultralow Phase Noise and Wideband CMOS VCO Using Symmetrical Body-Bias PMOS Varactors

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***Abstract*—This letter presents an ultralow phase-noise and wide turning-range CMOS voltage-controlled oscillator (VCO) for 5 GHz WLAN applications. The proposed PMOS-only VCO design with body-bias varactors achieves a tuning range of 20.4% and a phase noise of -138.4 dBc/Hz at 1 MHz offset. The total power consumption of the VCO core is 13.1 mW using a 1.8 V supply voltage. The achieved figure of merit with tuning range ($\mathrm{FOM_T}$) is -207.2 for the proposed CMOS VCO.**

***Index Terms*—Body bias, CMOS voltage-controlled oscillator (VCO), phase noise, PMOS varactor, tuning range.**

I. Introduction

FULLY integrated voltage-controlled oscillator (VCO) is an important and challenging building block in an RF transceiver. Many characteristics, such as tuning range, phase noise, power consumption and output power, must be considered in the design of a VCO for mobile device applications. Among these characteristics, phase noise most significantly impacts the signal quality in a communication system. Additionally, a wideband VCO design has multiband support, and excludes the possibility of ineffectiveness at the desired oscillation frequency due to the frequency shift caused by process variation.

Significant progress has been made recently in theories and analyses on the physical properties of CMOS VCOs as well as techniques for lowering the phase noise, owing to an improved understanding of the mechanism of phase noise. Pertinent literature cites increasing the quality factor (Q) value of LC tank as an effective means of reducing phase noise [1]. However, a high Q value narrows down the bandwidth, explaining that a balance must be found between phase noise and oscillation bandwidth. Using gm-boosting to increase the power of output signals is another common approach to optimize phase noise [2]. Additional active components are necessary for this circuit design, subsequently increasing noise level and thereby forming barriers to further improvement. Harmonic tuned LC tank [3] is also a common means of ameliorating the deterioration of phase noise caused by bias circuits. Although this approach employs additional filters for second harmonic suppression, the size of circuits and costs increase significantly. Switched inductors [4] or switched capacitors array [5] is widely used in wideband VCO design, where additional noise appears in [4] because of the use of MOS switches. Moreover, the P-N junction varactor used in [5] has a Q value that is too low. Above descriptions attest to the arduous challenges in designing a low-noise and wideband VCO. Recently, low-power VCO designs are prevalent [6]–[8], which faces more challenges to achieve low phase noise and wide tuning range.

This work designs a VCO at a center frequency around 5 GHz by using cross-coupled pairs of only PMOS [9]. Yet, in [9] the phase noise is not optimally reduced because of the use of tail current source in the differential stages. In this work, a design that optimizes phase noise is created by fully exploiting the unique characteristics of PMOS, in which very low frequency modulated (FM) flicker noise is achieved. Additionally, the deterioration of phase noise caused by the tail current source is prevented using a direct-bias design. As for the choice of tank circuit components, body-bias PMOS varactor is used to increase the tuning range of the VCO, meanwhile minimizing the flicker noise and its impact on the phase noise. Importantly, the proposed CMOS VCO design exhibits very low phase noise due to the PMOS-only and direct-bias circuit design.

II. Circuit Design

Fig. 1 shows the schematic of the proposed CMOS VCO. As summarized in Table I, compared to the conventional CMOS VCO designs that often use an NMOS-only or a complementary cross-coupled transistor pair, this design adopts a PMOS-only pair for reducing thermal and flicker noises in MOS devices [9]. Moreover, in the tank circuit, the body-bias PMOS varactors are employed instead of the common PN-junction varactors, thereby further improving the flicker noise while providing a wide tuning range [8], [9]. Also importantly, the proposed design utilizes a direct bias voltage rather than the most widely used mirrored bias current to avoid additional noise coupling from the tail current source transistors [10]. With all of the above design considerations, the circuit layout of the proposed CMOS VCO can be made fully symmetric, as can be seen in Fig. 2. The phase noise can therefore be reduced much more than is possible in a cross-coupled VCO architecture by minimizing the output amplitude and phase imbalance over a wide tuning range.

In this work, the design of LC-tank inductor incorporates the use of two individual spiral inductors with a guard ring attached around the edge. Using the guard ring increases the overall chip size; however, doing so reduces the mutual coupling between

Manuscript received October 23, 2012; revised January 02, 2013; accepted January 08, 2013. Date of publication January 23, 2013; date of current version February 08, 2013. This work was supported in part by the National Science Council of Taiwan under Grants 100-2221-E-110-081-MY3, 100-2221-E-110-082-MY3, 100-2622-E-110-001-CC1, and 101-2622-E-110-005-CC3.

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Digital Object Identifier 10.1109/LMWC.2013.2239635

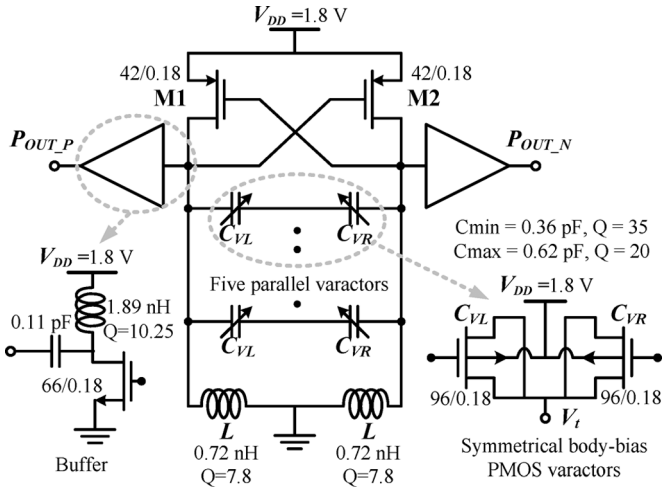

Fig. 1. Schematic of the proposed CMOS VCO.

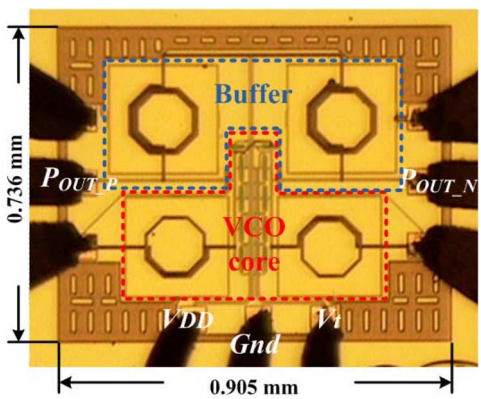

Fig. 2. Microphotograph of the designed 5 GHz 0.18 μm CMOS VCO.

TABLE I
COMPARISON OF DESIGN CONSIDERATIONS BETWEEN THE CONVENTIONAL AND PROPOSED CMOS VCOS

Design Consideration	Conventional CMOS VCO	Proposed CMOS VCO
Cross-coupled transistor pair	NMOS/ Complementary	PMOS
Varactor	PN junction	Body-bias PMOS
DC supply	Current mirror	Direct bias
Circuit layout	Not fully symmetric	Fully symmetric

inductors and its effect on the tank resonant frequency. Furthermore, the ring prevents the external noise entering the circuit through coupling from affecting the phase noise. Likewise, noise in LC-tank design is minimized by using only PMOS to construct the varactors. Nevertheless, the variable capacitance value in the conventional PMOS varactor design that consists of a PMOS transistor with the drain, source, and body connected together is too small to be wideband. In the varactor design of this work, the drain and source of the PMOS are shorted together to form one capacitor terminal while the polysilicon gate forms the other. Notably, the body is connected directly to V_{DD}. This structure, referred to herein as the "body-bias" structure, as shown in Fig. 1, maintains the operation of PMOS

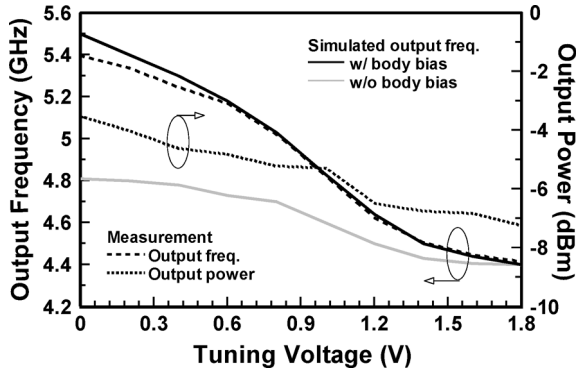

Fig. 3. Output frequency and power of the designed CMOS VCO.

within the inversion region rather than within the accumulation region. Therefore, even at the usual PMOS W/L ratio, a body-bias PMOS varactor can gain more than double the variable capacitance range than a conventional PMOS varactor. The proposed body-bias PMOS varactor is formed with 64 gate fingers, each finger having a gate length of 0.18 μm and a gate width of 1.5 μm. In Fig. 1, five pairs of symmetrical PMOS varactors are connected in parallel in the tank circuit. According to the simulation results, each pair of varactors varies the capacitance from 0.36 to 0.62 pF as a tuning voltage varies from 0 to 1.8 V. Therefore, the parallel connection of five pairs of varactors yields a capacitance range of 1.8 to 3.1 pF in the same tuning voltage range.

III. Results and Discussion

The demonstrated VCO was implemented using TSMC 0.18 μm 1P6M CMOS process technology, where the total chip size is 0.905×0.736 mm^2, including the bond pad, as shown in Fig. 2. The circuit performance was measured on a wafer using Cascade GSG RF probes with a 150 μm pitch. Spectra and phase noise levels were measured by an Agilent E5052B signal source analyzer (SSA). Fig. 3 compares the VCO tuning ranges. The solid line and the grey line represent the simulation results using PMOS varactors with and without the body bias. The VCO can significantly increase the tuning range up to 20.4%, if the body-bias PMOS varactors are chosen. The dashed line denotes the measurement results with the body-bias PMOS varactors, showing good agreement with simulation. Moreover, the measured output power as shown by the dotted line ranges from -7.2 to -3.5 dBm. In the measurement, a supply voltage of 1.8 V and a tuning voltage (V_t) of 1.8 V are provided by the SSA, capable of supporting a purer DC voltage than that of a conventional power supply. The oscillation frequency ranges from 5.4 to 4.4 GHz, as V_t varies from 0 to 1.8 V.

Fig. 4 shows the phase noise measurement results at 4.84 GHz, near the center frequency of the tuning range. The SSB phase noise measured at 10 kHz, 100 kHz, 1 MHz and 10 MHz offset from the carrier frequency was $-68.9, -111.6, -138.4$ and -158.3 dBc/Hz, respectively, exhibiting a f^{-4} noise below 100 kHz, a f^{-3} noise between 100 kHz and 1 MHz, and a f^{-2} noise above 1 MHz. It is noted that the SSA has an extremely low single sideband (SSB) phase noise sensitivity of -154 and -171 dBc/Hz at the offset frequency of 1 and 10 MHz, respectively. By using a 1.8 V

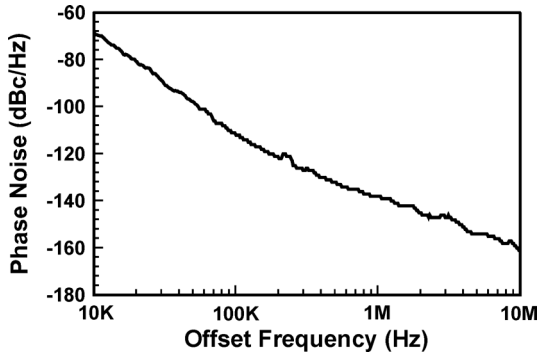

Fig. 4. Measured phase noise of the designed CMOS VCO operating at 4.84 GHz.

TABLE II
PERFORMANCE COMPARISON OF CMOS VCOS

Ref.	Process	Center Freq. (GHz)	P_{DC} (mW)	Tuning Range (%)	Phase Noise @1-MHz offset (dBc/Hz)	$\mathrm{FOM_T}$
[1]	0.35μm [a]	1.7	11	6.3	-142	-192.2
[2]	0.18μm	1.84	1.35	9.23	-126	-189.3
[3]	0.35μm	1	14.58	15	-132.4	-184.3
[4]	90 nm	11.75	7.67	61.9	-112	-200.4
[6]	0.18μm	3.1	1.57	20	-123	-196.9
[7]	0.13μm	22.8	1.4	7	-115	-197.6
[8]	0.18μm	5.15	0.96 [b]	29.12 [b]	-109.7 [b]	-193.4
[9]	0.35μm [a]	5.4	13.5	10.18	-117	-180.5
[10]	0.25μm	5.15	7.25	21	-123 [c]	-190.1
This work	0.18μm	5	13.1	20.4	-138.4	-207.2

[a] BiCMOS [b] Simulation [c] Reading from figure

supply voltage, the total power consumption of the VCO core is 13.1 mW.

Generally speaking, FM random walk (f^{-4}) noise is an enduring component in oscillator phase noise [11]. This component seems to be unnoticeable because the f^{-3}component, which is up-converted from the flicker noise in active devices and current sources, significantly outweighs FM random walk noise. However, since the proposed circuit design can reduce the flicker noise in MOSFET, the FM flicker (f^{-3}) noise is kept to a minimum. Consequently, the f^{-4} noise can be clearly seen in the phase noise measurement. Overall, the proposed CMOS VCO achieves both low phase noise and wide tuning range.

Table II summarizes the measured performance, where the figure of merits with tuning range $(\mathrm{FOM_T})$ [12] is used for comparison between this work and other state-of-the-art CMOS VCOs and given by

$$\mathrm{FOM_T} = L\{\Delta\omega\} + 10\log\left(\frac{P_{diss}}{1\,\mathrm{mW}}\right) - 20\log\left(\frac{\omega_0}{\Delta\omega}\cdot\frac{F_T}{10}\right) \quad (1)$$

where $L\{\Delta\omega\}$ denotes the phase noise in dBc/Hz at the offset angular frequency $\Delta\omega = 2\pi \times 10^6$ radian·Hz; P_{diss} is the dc power consumption in mW; ω_0 is the center angular frequency in radian·Hz; F_T is the frequency tuning range in percent. As Table I shows, the designed VCO has an $\mathrm{FOM_T}$ of -207.2, which is the best record among CMOS VCOs to the authors' knowledge.

IV. CONCLUSION

This work proposes a PMOS-only and direct-bias design of CMOS VCO with a fully symmetric structure to achieve an ultralow phase noise. Moreover, the body-bias PMOS varactors are used in the tank circuit to further reduce the flicker noise, and meanwhile increase the tuning range. Based on a phase noise of -138.4 dBc/Hz at 1 MHz offset, a tuning range of 20.4%, and a $\mathrm{FOM_T}$ of -207.2, our final circuit measurement results deliver one of the most remarkable performances in the current CMOS VCO designs.

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