Low-Noise and High-Linearity Wideband CMOS Receiver Front-End Stacked With Glass Integrated Passive Devices

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***Abstract*—This paper presents a stacked RF front-end (RFE) package for wideband receiver applications. While having a power consumption of 18 mW, the flipped CMOS chip consisting of a low-noise amplifier and a quadrature down-conversion mixer stacks on a glass integrated passive device (GIPD) substrate, subsequently achieving a noise figure of 2.2–2.8 dB and a conversion gain of 23–25 dB over 1–6 GHz. Moreover, the RFE package uses a GIPD balun with a high common-mode rejection ratio and a post-distortion linearizer in the CMOS mixer, subsequently resulting in an IIP_2 of 57–68 dBm and an IIP_3 of -5.2–-3.5 dBm over the entire operating band. This paper also elucidates how coupling between the flipped CMOS chip and GIPD balun affects the RFE linearity. Fabricated with 0.18-μm CMOS technology, the flipped CMOS chip is packaged on the GIPD substrate with a footprint area of 1.8×1.8 mm^2.**

***Index Terms*—CMOS receiver, glass integrated passive device (GIPD), stacked RF front-end (RFE) package, wideband receiver.**

I. Introduction

FOR ADVANCED wireless communication systems, a universal software-defined radio (SDR) provides a tunable platform over a wide frequency range. The popular SDR platforms encompass a multi-band/multi-standard system ranging from 1 to 6 GHz. To achieve a receiver RF front-end (RFE) operating for the multi-band/multi-standard system, a wideband solution is more flexible and less complex than a combination of multiple narrowband ones for system-on-chip (SoC) integration [1]–[3]. However, this preference poses stringent requirements on the RFE, such as a low noise figure (NF) and high linearity over a wide frequency range [4], [5].

Despite its wide use in a wideband RFE due to its high integration and low power consumption, direct-conversion architecture confronts some design challenges such as a low output dc offset and a high linearity characterized by input second- and third-order intercept points (IIP_2 and IIP_3). A double-balanced down-conversion mixer can generally decrease an output dc offset, owing to its low local oscillator (LO) self-mixing and second-order intermodulation distortion (IMD). Fig. 1 illustrates several wideband direct-conversion RFE architectures. The block diagrams of these architectures commonly consist of a wideband low-noise block (LNB) and a wideband in- and quadrature-phase (I/Q) demodulator. The LNBs used in them are different and may be classified as Type-I [1], [2], Type-II [3], and Type-III [6]. Type-I has the most compact chip size than the other types when a wideband balun low-noise amplifier (referred to as balun-LNA) is used in an LNB. Nevertheless, a balun-LNA might suffer from an inferior balanced output signal, degrading IIP_2 in the subsequent stage. In addition, the balun-LNA exhibits an NF of more than 3 dB below 6 GHz [7]. Conversely, using a wideband passive balun, which possesses high common-mode rejection ratio (CMRR) and consumes no dc power in Type-II significantly mitigates IIP_2 degradation of the subsequent stage. However, this design must occupy a large chip size when integrating this bulky passive component in an SoC. What is more, the integrated passive balun with a low quality (Q) factor that precedes a low-noise amplifier (LNA) significantly aggravates the NF of a wideband receiver. Despite Type-III having a superior NF to that of Type-I and Type-II, owing to the removal of RF balun at the receiver input, the disadvantages of integrating a passive balun in an SoC is the same as those of Type-II.

This paper proposes a low-noise and high-linearity wideband flip-chip CMOS RFE stacked with glass integrated passive devices (GIPDs). In the past, a number of GIPD designs have been

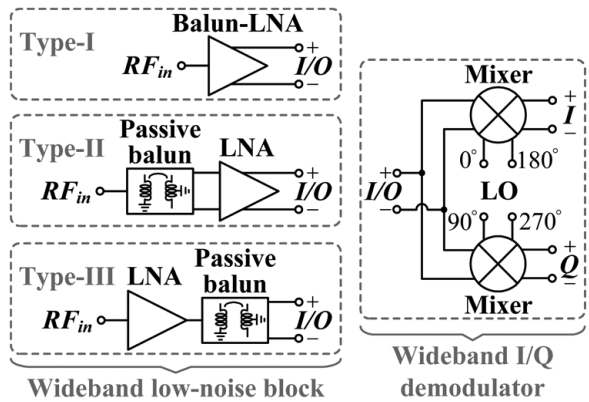

Fig. 1. Three common types of wideband direct-conversion RFE architectures.

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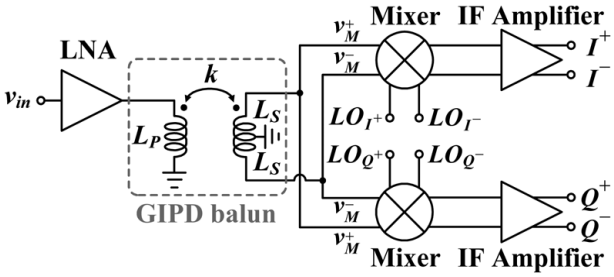


Fig. 2. Proposed wideband CMOS RFE with a GIPD balun.

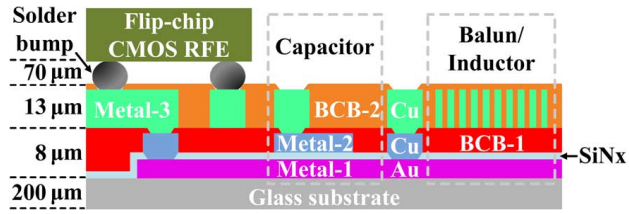


Fig. 3. Cross section of GIPD and flip-chip CMOS technologies.

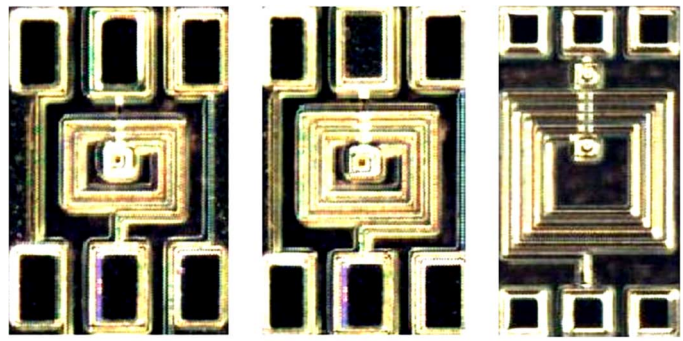


Fig. 4. GIPD inductor testkeys with metal width of 10 μm and metal space of 10 μm. (a) N25 with vertical outside dimension (OD_V) of 185 μm and horizontal outside dimension (OD_H) of 228 μm. (b) N35 with OD_V of 224 μm and OD_H of 268 μm. (c) N45 with OD_V of 320 μm and OD_H of 320 μm.

proposed for RFE applications [8]–[10]. In [8], the performance of the bandpass filter and diplexer using GIPD technology was investigated and compared with those using silicon and low-temperature co-fired ceramic (LTCC) technologies. Recently, parametric designs of a Marchand balun [9] and balun bandpass filter [10] using GIPD technology were developed based on a modeling approach. Previous works [11]–[13] also used integrated passive devices (IPDs) with a high Q-factor in individual RF active circuitry to improve various performances such as chip size, phase noise, and NF. For receiver system integration, GIPD baluns were used at the RF and LO inputs of a CMOS RFE [14], [15], but unfortunately, these integration techniques are suitable for narrowband applications, and their placing the GIPD balun at the RF input is detrimental to the NF. In this paper, using GIPD and flip-chip technologies not only improves RF performance of a wideband RFE, but also achieves a compact RFE module size by vertical stacking of the CMOS chip and GIPDs. This paper also elucidates how coupling between the flipped CMOS chip and GIPD balun affects the RFE linearity. Furthermore, an attempt is made to improve linearity of a wideband RFE by using a post-distortion (PD) linearizer in the wideband I/Q demodulator.

II. Wideband RFE Architecture

Fig. 2 illustrates the proposed wideband RFE architecture. A wideband single-ended LNA is adopted to avoid the need of an RF input balun and reduce power consumption as well as chip size. Importantly, IIP_2 is critical for a wideband direct-conversion RFE because the related second-order IMD caused by in-band interference often desensitizes the baseband detection [4]. In general, a double-balanced down-conversion mixer can be used to reduce this effect, and therefore a balun between a single-ended LNA and a wideband I/Q demodulator is necessary for performing single-to-differential conversion.

Despite having a dense CMOS integration, a wideband active balun exhibits a lower CMRR than that of a wideband passive balun [16]. This feature significantly degrades the IIP_2 of a down-conversion mixer because the imbalanced amplitude and phase occur in the differential RF input signal [17]. However, although an on-chip passive balun has a high CMRR over a wide frequency range [18], [19], its bulky winding makes it difficult to be integrated into an SoC when an RFE operates below 6 GHz. In contrast, a flipped CMOS chip stacked above a GIPD balun with a high Q-factor is proposed in this study. It can thereby achieve a compact CMOS chip size and meanwhile avoid the undesired silicon substrate noise coupling through the CMOS inductive components [20].

Fig. 3 shows the cross section of GIPD and flip-chip CMOS technologies. Metal-1 and Metal-3, which are used to fabricate inductors and balun, are the 3-μm-thick layer of aurum (Au) and 10-μm-thick layer of copper (Cu), respectively. Metal-2, which has a 3-μm-thick layer of Cu, is used exclusively for the bottom electrodes of capacitors. The bypass capacitors for supply noise filtering are fabricated using GIPD technology. RF signals and dc biases between the flipped CMOS chip and GIPD substrate are connected by using solder bumps, which have a diameter of 100 μm. To achieve a compact stacked RFE package size, the flipped CMOS chip fully covers the GIPD balun.

In this study, the designs of GIPD inductors and balun are performed using Ansys' High Frequency Structure Simulator (HFSS). Fig. 4 illustrates GIPD inductor testkeys, which are 2.5 turns (referred to as N25), 3.5 turns (referred to as N35), and 4.5 turns (referred to as N45), respectively. Fig. 5 illustrates the simulated and measured inductances, as well as Q-factors of these inductor testkeys. It is seen from this figure that the simulation and measurement results correlate well with each other. Generally speaking, with the help of high-Q GIPDs, the power consumption of the CMOS circuit can be less wasted on compensating for the inferior RF performance caused by low-Q CMOS passive devices. Furthermore, the production cost of GIPDs may be lower because the fabrication process involves only the metal layers on the glass surface. Due to high Q-factor and low production cost, GIPDs have become more and more popular for RF system-in-package applications.

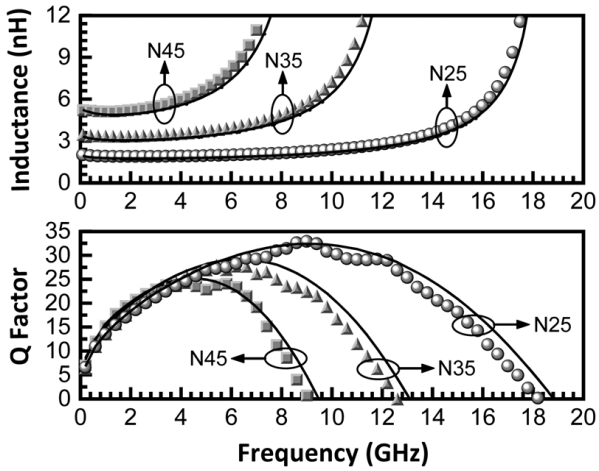
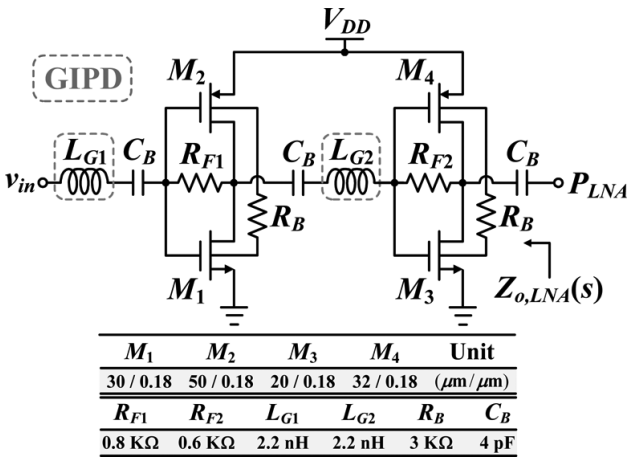


Fig. 5. Simulated and measured inductance (*upper*), as well as Q-factor (*lower*) of N25, N35, and N45. Notably, solid lines denote simulated results, and symbols (square, triangle, and circle) denote measured results.



M_1	M_2	M_3	M_4	Unit
30 / 0.18	50 / 0.18	20 / 0.18	32 / 0.18	(μm/μm)
R_{F1}	R_{F2}	L_{G1}	L_{G2}	R_B	C_B
0.8 KΩ	0.6 KΩ	2.2 nH	2.2 nH	3 KΩ	4 pF

Fig. 6. Circuit schematic of the LNA with GIPD inductors.

III. Circuit Designs

A. Wideband Low-Voltage LNA With GIPD Inductors

From an RF link budget design perspective, the performance of an LNA dominates the receiver sensitivity. Therefore, a wideband LNA must feature input matching to an RF source impedance R_S of 50 Ω, flat gain, and low NF over a wide frequency range. Fig. 6 illustrates the design of the proposed wideband low-voltage LNA. The circuit schematic shown in Fig. 6 includes a driver stage and a buffer stage. The former comprises transistors M_1 and M_2 with a gate width of 30 and 50 μm, respectively. The latter is composed of transistors M_3 and M_4 with a gate width of 20 and 32 μm, respectively. Using a GIPD inductor N25 with a value of $L_{G2} = 2.2$ nH substantially improves the interstage matching between the driver and buffer stage. Notably, the parasitic effects of connecting to the GIPD inductor are considered in this interstage matching. Moreover, the threshold voltage V_T of $M_1 - M_4$ is lowered using the self-forward body-bias technique, thereby reducing the supply voltage V_{DD}.

Despite occupying a small chip size, a complementary LNA without an input series inductor L_{G1} suffers from a stringent tradeoff between input and noise matching. According to Fig. 7, the simulated minimum NF $\mathrm{NF}_{\min}$ and the maximum input reflection coefficient $|S_{11,max}|$ for the LNA without L_{G1} strongly depend on the feedback resistor R_{F1} within 1–6 GHz. Therefore, to achieve an input matching of below −10 dB over 1–6 GHz, another N25 inductor with $L_{G1} = 2.2$ nH is used to reduce the input mismatching at higher frequencies when using an R_{F1} of 800 Ω to achieve an NF below 2.4 dB, as shown in Fig. 7. The lower plot of Fig. 8 indicates that the input reflection coefficient $|S_{11}|$ of below −10 dB over 1–6 GHz is achieved when using L_{G1}. Without considering the noise contributed by the buffer stage, noise factor F of the LNA with L_{G1} is derived as

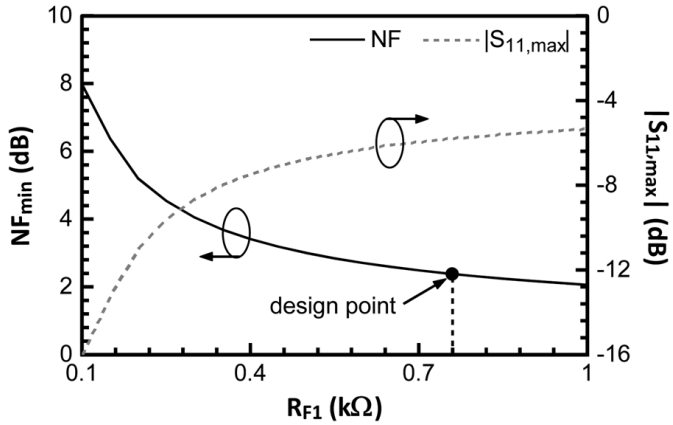


Fig. 7. Simulated $\mathrm{NF}_{\min}$ and $|S_{11,max}|$ of the LNA without L_{G1} versus different R_{F1} values.

$$F \approx 1 + \frac{R_G}{R_S} + \frac{(R_{F1} + 2R_L)^2}{R_{F1}R_L^2(1+Q_G^2)G^2R_S} + \frac{\gamma}{\alpha\,(1+Q_G^2)\,R_SG} \tag{1}$$

where R_G, R_L, Q_G, G, γ, and α are the parasitic resistance of L_{G1}, input impedance of buffer stage, Q-factor of L_{G1}, equivalent transconductance of driver stage, thermal noise coefficient of transistor, and ratio of transconductance g_m to zero-bias drain conductance, respectively. Equation (1) indicates that Q_G dominates the F of the LNA when G and R_{F1} are designed for input and noise matching.

The LNA consumes 3.8 mW from a 1.5-V supply. The upper plot of Fig. 8 reveals that the NF of the LNA with L_{G1} is lower than that of the LNA without L_{G1}, due to the improvements of input and noise matching. In this figure, the LNA with GIPD L_{G1} exhibits a lower NF than that of the LNA with CMOS L_{G1}. This finding is attributed to the use of GIPD L_{G1} with a higher Q_G value of 17–24 within 1–6 GHz. Additionally, L_{G1} also forms a gain peak at higher frequencies, subsequently extending the 3-dB gain bandwidth of LNA [21].

B. Down-Conversion Mixer With a PD Linearizer

Fig. 9 illustrates the circuit schematic of the proposed common-gate (CG) double-balanced Gilbert mixer. The transconductance (referred to as G_m) stage comprises transistors M_5 and M_6. Basically, it uses a capacitive cross-coupled common-gate (CCC-CG) topology to boost the capabilities of current-driving and noise suppression [22]. In this stage,

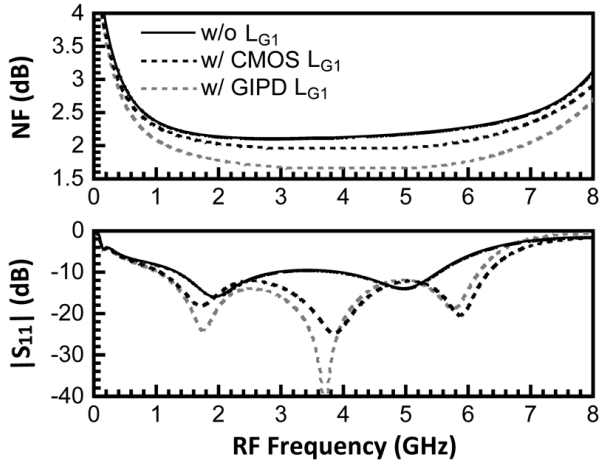
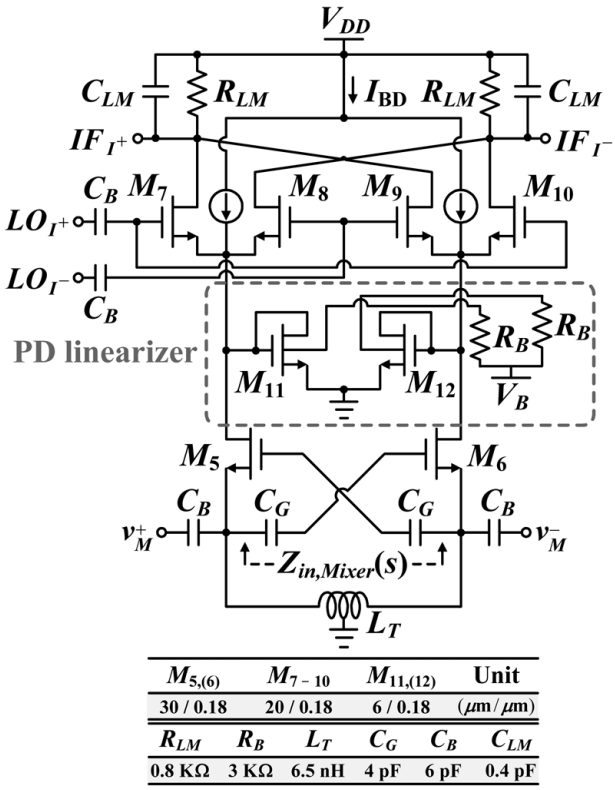


Fig. 8. Simulated NF (*upper*) and $|S_{11}|$ (*lower*) of the LNA for comparison with and without L_{G1} in which L_{G1} is an GIPD or CMOS inductor with a value of 2.2 nH.



$M_{5,(6)}$	M_{7-10}	$M_{11,(12)}$	Unit
30 / 0.18	20 / 0.18	6 / 0.18	(μm/μm)
R_{LM}	R_B	L_T	C_G	C_B	C_{LM}
0.8 KΩ	3 KΩ	6.5 nH	4 pF	6 pF	0.4 pF

Fig. 9. Circuit schematic of a single down-conversion mixer with a PD linearizer without showing output IF amplifier and bias circuits.

a symmetric center-tap inductor L_T is used to resonate with the gate–source capacitance of M_5 and M_6. Owing to its high inductance, the routing complexity and area of occupation are major issues in choosing an appropriate implementation technology for this inductor. In this work, the L_T inductor was finally realized in CMOS rather than GIPD process based on a thorough consideration of these issues.

The switching stage comprising transistors $M_7 - M_{10}$ are biased near V_T of a transistor to diminish the noise contribution caused by nonideal switching. Meanwhile, utilizing the PD linearizer comprising transistors M_{11} and M_{12} further

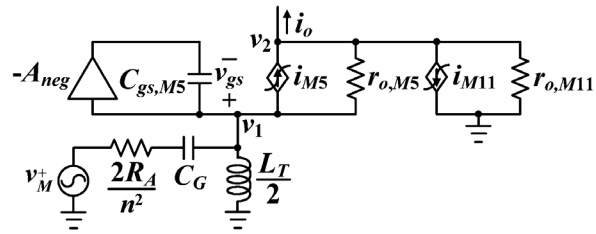


Fig. 10. Nonlinear equivalent half-circuit of a combined G_m stage and PD linearizer in which the gate–source capacitance of M_{11} is neglected due to small device size. The negative feedback gain $A_{\rm neg}$ is equal to unity due to that C_G is much larger than $C_{{\rm gs},M5}$.

enhances IIP_2 and IIP_3 of the mixer. Furthermore, a differential common-source (CS) IF amplifier, which is not shown in Fig. 9, cascades after the mixer. The maximum available IF bandwidth of this mixer, limited to the *RC* time constant of the load resistance and capacitance, is about 300 MHz.

Generally speaking, the G_m stage dominates the linearity of a mixer. Empirically, the second-order nonlinearity of the G_m stage degrades the IIP_2 of a mixer when device mismatch or differential imbalance exist [17]. The PD linearizer, which has a low noise contribution, has been used in [23] to improve the linearity of an LNA. Similarly, this work uses a PD linearizer to improve the linearity of the mixer G_m stage and subsequently enhance IIP_2 and IIP_3 of the mixer. Fig. 10 shows the nonlinear equivalent half-circuit of a combined G_m stage and PD linearizer in which R_A is the real part of output impedance of the LNA, and n^2 is the primary to secondary inductance ratio L_P/L_S of the transformer. Accordingly, the source resistance in this half-circuit is set at $2R_A/n^2$. In Fig. 10, the drain current i_{M11} of M_{11} partially cancels the drain current i_{M5} of M_5. Consequently, the IMD output currents of M_5 can also be cancelled by those of M_{11}. With Taylor-series expansion, the nonlinear drain currents of M_5 and M_{11} are expressed as

$$i_{M5} = 2g_1 v_1 + 4g_2 v_1^2 + 8g_3 v_1^3 \tag{2}$$

$$i_{M11} = g_{1c} v_2 + g_{2c} v_2^2 + g_{3c} v_2^3 \tag{3}$$

$$v_2 = c_1 v_1 + c_2 v_1^2 + c_3 v_1^3 \tag{4}$$

where g_i and g_{ic} are the ith-order transconductance of M_5 and M_{11}, respectively, in which g_1 equals g_m of M_5, and c_i is the ith-order impedance ratio of drain to source of M_5. With the help of Volterra series, the second- and third-order IMD output currents of the combined G_m stage and PD linearizer are given as

$$i_{o,\mathrm{2nd}} = A_1(s)^2 \left[4g_2 - c_1^2 g_{2c} - g_{2o,\mathrm{eff}} g_{m,\mathrm{eff}} H(\Delta s)^{-1}\right] v_{\mathrm{in}}^2 \tag{5}$$

$$\begin{aligned} i_{o,\mathrm{3rd}} = {} & A_1(s)^3 \Bigg\{ 8g_3 - c_1^3 g_{3c} - g_{m,\mathrm{eff}} \left(c_1^3 g_{3c} + \frac{8 g_3 r_{o,M5}}{r_{o,M11}} \right) H(s)^{-1} \\ & + \frac{2}{3} g_{2o,\mathrm{eff}}^2 g_{m,\mathrm{eff}} \left[2H(\Delta s)^{-1} + H\left(\sum s\right)^{-1} \right] \\ & \times H(s)^{-1} - \frac{2}{3} \left(16 g_2^2 - c_1^4 g_{2c}^2\right) H\left(\sum s\right)^{-1} \Bigg\} v_{\mathrm{in}}^3 \end{aligned} \tag{6}$$

where

$$A_1(s) = \frac{n^2}{2R_A H(s)}\left(1 + \frac{r_{o,M5}}{r_{o,M11}}\right) \tag{7}$$

$$g_{m,\text{eff}} = (2g_1 - c_1 g_{1c}) \tag{8}$$

$$g_{2o,\text{eff}} = \left(c_1^2 g_{2c} + \frac{4g_2 r_{o,M5}}{r_{o,M11}}\right) \tag{9}$$

$$H(s) = \left[Y(s) + \frac{n^2}{2R_A}\right]\left(1 + \frac{r_{o,M5}}{r_{o,M11}}\right) + \left(\frac{1 + 2g_1 r_{o,M5}}{r_{o,M11}}\right) + c_1 g_{1c} \tag{10}$$

$$Y(s) = 2(sL_T)^{-1} + sC_{\text{gs},M5,(6)} + 2\left[\left(1 + Q_S^2\right) R_T\right]^{-1} \tag{11}$$

and parameters Δs and Σs denote the difference and sum frequencies of a two-tone signal, respectively. In (11), R_T and Q_S are parasitic resistance of L_T and series Q-factor of L_T, respectively. Since the factor $Y(s) + n^2/2R_A$ in (10) is a low-Q resonant response, $H(s)$ and $H(\Sigma s)$ exhibit a weak frequency-dependent characteristic within the operating frequency range, resulting in a wide linearization bandwidth. Moreover, the ratio $r_{o,M5}/r_{o,M11}$ is negligible due to that M_{11} is biased at a much lower drain current than M_5. Furthermore, the effects of $H(\Delta s)^{-1}$ and $H(\Sigma s)^{-1}$ are ignored if Δs and Σs are far away from the resonant frequency. Therefore, according to (5) and (6), $i_{o,2\text{nd}}$ and $i_{o,3\text{rd}}$ are cancelled when g_2 and g_3 are set equal to $c_1^2 g_{2c}/4$ and $c_1^3 g_{3c}[1 + g_{m,\text{eff}}/(n^2/2R_A + c_1 g_{1c})]/8$, respectively, in the resonant frequency. Nevertheless, the PD linearizer slightly degrades conversion gain and NF of the mixer, owing to the reduction of effective transconductance $g_{m,\text{eff}}$ given in (8) of M_5. Therefore, the PD linearizer should be biased in a low drain current region to achieve the cancellation conditions of $i_{o,2\text{nd}}$ and $i_{o,3\text{rd}}$ without substantially sacrificing gain and NF of the G_m stage. Accordingly, M_{11} and M_{12} with a gate width of 6 μm are set to obtain an optimum design between conversion gain and linearity. Additionally, body-biasing voltage V_B is applied to M_{11} and M_{12} for trimming the g_{2c} and g_{3c} values, thus assisting to cancel $i_{o,2\text{nd}}$ and $i_{o,3\text{rd}}$.

The G_m stage that uses the CCC-CG topology has an input conductance equal to $2g_m$ [22]. This input conductance is further set equal to the source conductance $n^2/2R_A$ for achieving input impedance matching. Under this matching condition, the noise factor F of a single mixer excluding the PD linearizer is derived as

$$F = 1 + \frac{9}{g_m R_{\text{LM}}} + \frac{\gamma}{\alpha}\left(\frac{18 I_S}{g_m \pi A_{\text{LO}}} + 2\right) + \frac{2R_A}{(Q_s n)^2 R_T} \tag{12}$$

where R_{LM}, I_S, and A_{LO} are the output load of the mixer, the bias current of $M_7 - M_{10}$, and the amplitude of the LO signal, respectively. Injecting a current-bleeding current I_{BD} into the switching stage of the mixer shown in Fig. 9 moderately reduces I_S and meanwhile enlarges R_{LM} without depressing voltage headroom of the switching stage, thereby improving conversion gain [24]. Equation (12) indicates that the reduced I_S and enlarged R_{LM} further improves the NF. To make a good tradeoff among the conversion gain, NF, and linearity, M_5 and M_6 with a gate width of 30 μm, $M_7 - M_{10}$ with a gate width of 25 μm, and R_{LM} of 800 Ω are set, respectively.

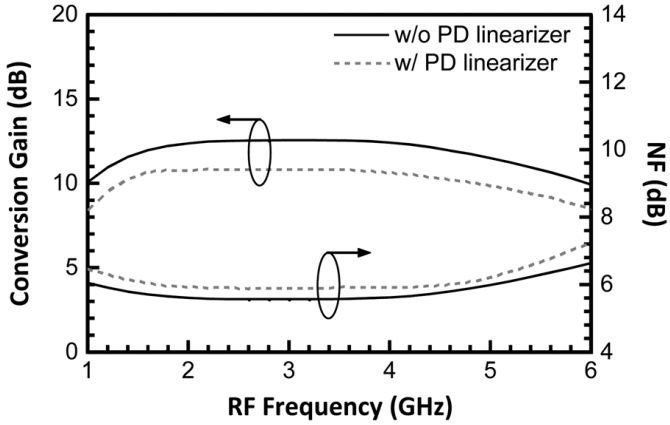


Fig. 11. Simulated conversion gain and NF of a single mixer with and without a PD linearizer.

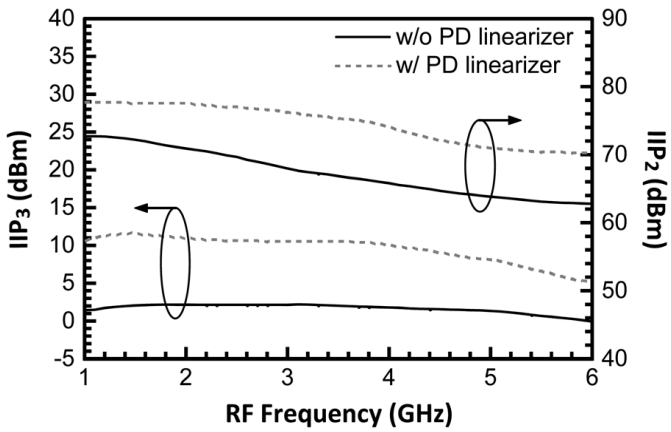


Fig. 12. Simulated IIP_2 and IIP_3 of a single mixer with and without a PD linearizer.

The mixer with an output IF amplifier dissipates 7.1 mW at a supply voltage of 1.8 V. Fig. 11 compares the simulated conversion gain and NF of a single mixer with and without a PD linearizer. As can be seen in the entire operating band, the conversion gain of a single mixer with a PD linearizer exhibits a maximum degradation of 1.7 dB compared to a single mixer without a PD linearizer. This finding is due to the reduction of $g_{m,\text{eff}}$. Meanwhile, the NF of a single mixer with a PD linearizer is slightly degraded due to a similar reason. Fig. 12 shows the simulated IIP_2 and IIP_3 of a single mixer with an ideal balun at the RF input. In this simulation, the post-layout effects on the design performance are included using Agilent Momentum simulator. According to the simulation results, the IIP_2 and IIP_3 of a single mixer with a PD linearizer exhibit a maximum improvement of 10 dB compared to a single mixer without a PD linearizer.

C. Bifilar Transformer-Based GIPD Balun

The bifilar transformer-based balun, which has a high CMRR over a wide frequency range due to its symmetric structure, is used in this work. This balun is fabricated with GIPD technology, thus obtaining a high Q-factor. To achieve maximum gain transformation, the interstage matching of cascaded LNA, balun, and I/Q demodulator must be designed

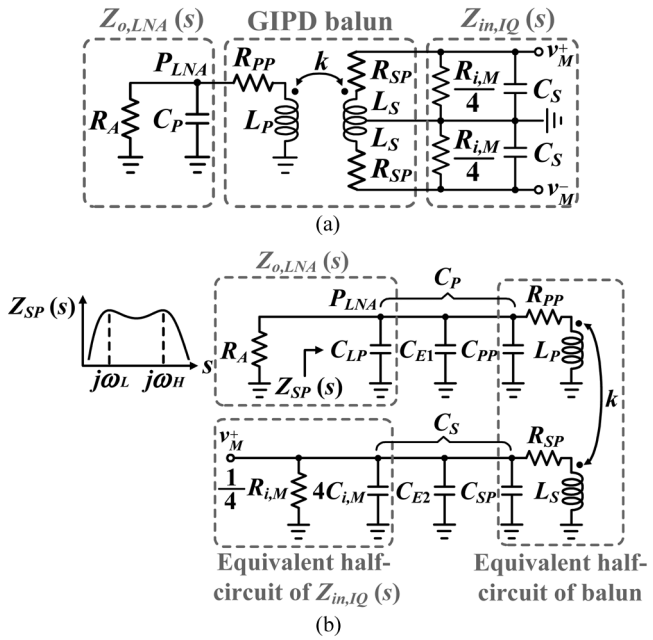


Fig. 13. Equivalent cascaded circuits. (a) Simplified full schematic. (b) More detailed schematic with parasitic capacitances and half-circuits for differential operation.

carefully. Fig. 13(a) illustrates the equivalent cascaded circuit. According to Fig. 13(a), the GIPD balun serves as the output load of LNA in which R_A is the real part of equivalent output impedance $Z_{o,\mathrm{LNA}}(s)$ of the LNA; k represents the magnetic coupling coefficient of the GIPD balun; L_P refers to the primary inductance of the GIPD balun; L_S denotes the secondary inductance of GIPD balun in an equivalent differential half-circuit; C_P represents the primary capacitances including the parasitic capacitance C_{PP} of primary winding, the equivalent output capacitance C_{LP} of the LNA, and the shunt metal–insulator–metal (MIM) capacitor C_{E1}; C_S denotes the secondary capacitances, including the parasitic capacitance C_{SP} of secondary winding, the shunt MIM capacitor C_{E2}, and the input capacitance $C_{i,M}$ of the I/Q demodulator in an equivalent differential half-circuit; and R_{PP} as well as R_{SP} represent the parasitic resistances of L_P and L_S, respectively.

According to Fig. 13(a), the secondary winding of the GIPD balun connects with the I/Q demodulator, in which $Z_{\mathrm{in,IQ}}(s)$ is the differential equivalent input impedance of the I/Q demodulator, and $R_{i,M}$ represents the real part of the differential input impedance $Z_{\mathrm{in,Mixer}}(s)$ of a single mixer. For a mixer in CCC-CG topology, $Z_{\mathrm{in,Mixer}}(s)$ is expressed as [22]

$$Z_{\mathrm{in,Mixer}}(s) = \left[\frac{g_{m,\mathrm{eff}} + Y(s)}{2}\right]^{-1} \tag{13}$$

where $g_{m,\mathrm{eff}}$ is given in (8). Significantly, the interstage matching of cascaded stages can be achieved by designing the GIPD balun, owing to that the proposed bifilar transformer-based GIPD balun has an impedance transformation between primary and secondary windings. Fig. 13(b) illustrates the equivalent cascaded circuit with parasitic capacitances and a differential half-circuit, in which the GIPD balun is modeled as a coupling of two parallel resonant circuits L_PC_P and

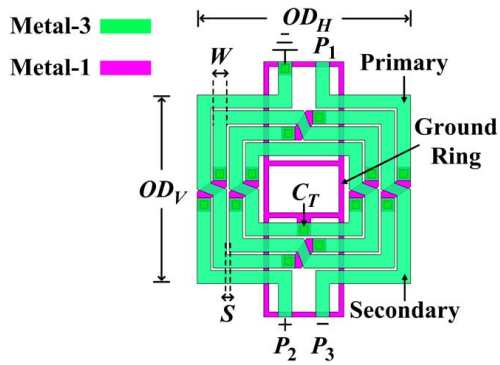


Fig. 14. Proposed bifilar transformer-based GIPD balun.

L_SC_S with an equivalent input impedance $Z_{SP}(s)$. Therefore, the bandwidth of $Z_{SP}(s)$ can be designed by tuning resonant frequencies ω_L and ω_H, which are given as [25]

$$\omega_{L,H} = \omega_o\sqrt{1 \pm k}\Big|_{L_PC_P = L_SC_S} \tag{14}$$

where ω_o denotes the resonant frequency of a single resonator. The transformer ratio n^2 at the resonant frequencies ω_L and ω_H is expressed as

$$n^2 \equiv \frac{L_P}{L_S} = \frac{\mathrm{Re}\left[Z_{o,\mathrm{LNA}}(s)\right]}{\mathrm{Re}\left[\frac{Z_{\mathrm{in,IQ}}(s)}{2}\right]} = \frac{4R_A}{R_{i,M}}\Bigg|_{s=j\omega_{L,H}}. \tag{15}$$

Equation (15) represents the interstage matching condition for the maximum gain transmission between cascaded stages. A transformer ratio n^2 of 2 is used for a given $R_{i,M} = 2R_A$. The resonant frequencies ω_L and ω_H of the GIPD balun are obtained by designing the k value given in (14), but a tradeoff between the desired bandwidth and in-band ripples must be considered beforehand [25]. In this study, the primary and secondary windings of the GIPD balun are set at two turns each. Accordingly, L_P of 3.5 nH, L_S of 1.7 nH, C_{E1} of 0.5 pF, C_{E2} of 1.5 pF, and k of 0.65 are designed, respectively.

Fig. 14 shows the proposed bifilar transformer-based GIPD balun in which P_1 is the input port of primary winding; P_2 and P_3 are the differential output ports of secondary winding; the horizontal outside dimension (OD_H) is 852 μm; the vertical outside dimension (OD_V) is 762 μm; the metal width W is 50 μm; and the metal spacing S is 10 μm. In Fig. 14, the center tap C_T of secondary winding is connected to a common ground. With the help of Ansys' HFSS, this common ground adopts a symmetric three-frame pattern to obtain a higher self-resonant frequency and meanwhile maintain a high CMRR at higher frequencies.

D. Stacked RFE With Consideration of Coupling Effects

In CMOS fabrication, the dummy metal (DM) fill required by chemical mechanical polishing (CMP) process must meet the CMOS metal density rules. However, the generation of an eddy current significantly influences the performance of an inductor with underneath DMs [26]. Therefore, a flipped CMOS inductor coupled with underneath metal markedly degrades the Q-factor and self-inductance [27]. In this work, the GIPD inductors are placed without overlapping with the flip-chip CMOS RFE to

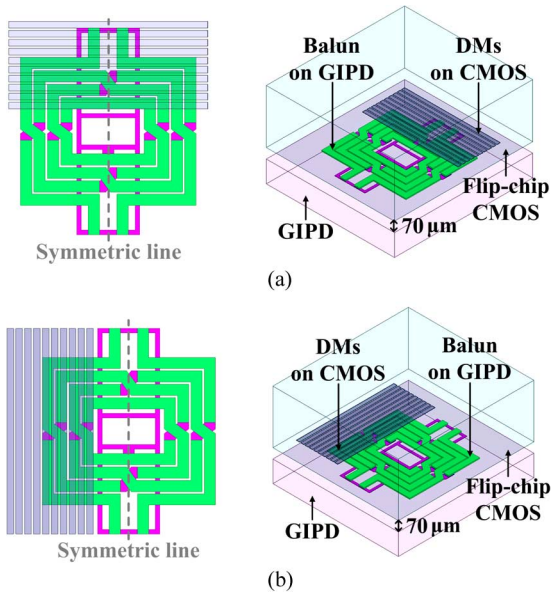


Fig. 15. Electromagnetic (EM) simulation model of the flipped CMOS chip stacked above the GIPD balun. (a) Flipped CMOS chip with symmetric DMs. (b) Flipped CMOS chip with asymmetric DMs.

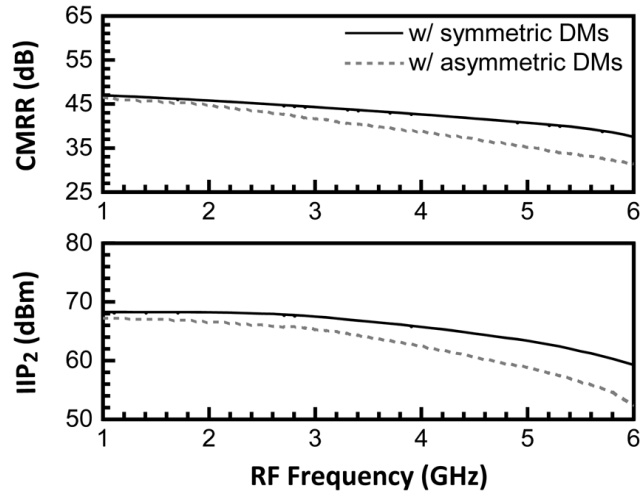


Fig. 16. Simulated CMRR of GIPD balun versus different CMOS DMs structures (*upper*) and simulated IIP_2 of cascaded LNA, balun, and I/Q demodulator versus different CMOS DMs structures (*lower*).

avoid a considerable change in their electrical characteristics. In contrast, the flipped CMOS chip fully covers the GIPD balun, and therefore the effect of coupling between the GIPD balun and flipped CMOS DMs must be addressed.

Fig. 15 illustrates the Ansys HFSS simulation model of the flipped CMOS chip stacked above the GIPD balun in which only Metal-6 of Al-Cu with 2.34-μm thickness and Metal-5 of Al with 0.53-μm thickness are used as CMOS DMs for simplifying the simulation model. Moreover, since the effect of CMOS DMs on the GIPD balun is capacitive at the frequency range of interest, metal lines can serve as good approximation of the lines of small metal rectangles that are commonly used in practical DM fill patterns.

Fulfilling the CMP process requirement generally involves two layout types of CMOS DMs, which are the flipped CMOS chip with symmetric DMs [see Fig. 15(a)] and asymmetric DMs [see Fig. 15(b)]. The upper plot of Fig. 16 compares the simulated CMRRs of the GIPD balun stacked below the flipped CMOS chip with symmetric and asymmetric DMs. Obviously, the flipped CMOS chip with asymmetric DMs significantly decreases the CMRR of the GIPD balun at higher frequencies.

As shown in Fig. 2, the proposed wideband CMOS RFE consists of an LNA and a quadrature down-conversion mixer that includes a pair of mixers with output IF amplifiers. The total estimated power consumption is 18 mW in simulation. To perform circuit co-simulation, the simulated S-parameters of the GIPD balun stacked below the flipped CMOS chip with symmetric and asymmetric DMs are obtained by Ansys' HFSS, while the small-signal S-parameters of the LNA and mixer including post-layout parasitics are generated using Agilent Technologies' Advanced Design System (ADS) and Momentum simulators. The lower plot of Fig. 16 shows the IIP_2 co-simulations of the cascaded LNA, balun, and I/Q demodulator. Obviously, the GIPD balun stacked below the flipped CMOS chip with symmetric DMs achieves a maximum IIP_2 improvement of 6.5 dB at 6 GHz when compared to that with asymmetric DMs.

IV. Experimental Results

In the implementation of the stacked RFE package, the flipped CMOS chip with a size of 1×1 mm^2 was fabricated using the 0.18-μm RF CMOS one-poly-six-metal (1P6M) technology. The external passive components include the two 2.5-turn spiral inductors and one two-turn bifilar transformer balun. They were all realized on a 1.8×1.8 mm^2 GIPD substrate. In the simulation, the parasitics of bondwires, RF pads, and solder bumps are taken into account. Fig. 17(a)–(d) illustrates the chip micrographs of the proposed wideband CMOS RFE. To prevent the GIPD balun from significant performance degradation, CMOS devices and DMs should not be placed underneath the inner opening of the GIPD balun, as shown in the empty region denoted by D in Fig. 17(a). Moreover, the symmetric CMOS DMs layout shown in Fig. 15(a) is adopted to avoid a quick drop in the CMRR of the GIPD balun at higher frequencies. Notably, a GIPD inductor N45 with a value of $L_{\mathrm{Test}} = 6$ nH, shown in Fig. 17(b), is used for dc testing. To achieve a compact package size, the flipped CMOS chip fully covers the GIPD balun, as shown in Fig. 17(c). Fig. 17(d) shows a side view of the implemented stacked RFE package.

The stacked RFE package was wire-bonded to a 0.8-mm-thick FR4 board for measurement purpose. During the measurement, the external LO and IF baluns with impedance transformation ratio of 1:2 were used to convert between single-ended and differential signals. In addition, the tentative IF frequency is 20 MHz and the LO power of about -6 dBm was set by a signal generator with a four-way quadrature power divider. As a measurement result, the stacked RFE package consumes a dc power of 18 mW. Fig. 18 demonstrates the simulated and measured $|S_{11}|$ of the stacked RFE package. Measurement results indicate that a $|S_{11}|$ below -10 dB covers a frequency range of 1–6 GHz. Fig. 19 shows the measured results of port-to-port isolation. Owing to the use of the GIPD balun, the reduction

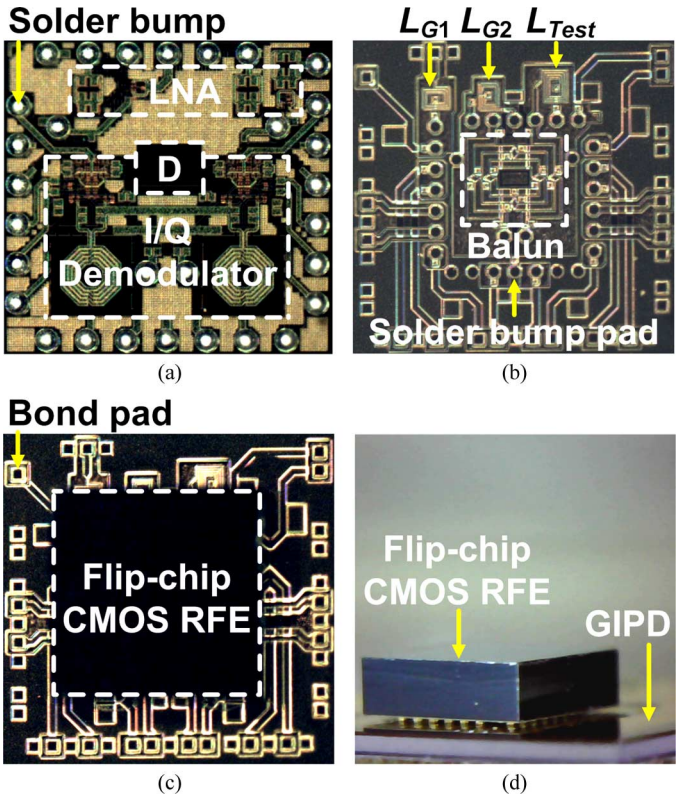


Fig. 17. Chip micrographs. (a) 1 × 1 mm^2 CMOS chip including solder bumps. (b) 1.8 × 1.8 mm^2 GIPD chip including bond pads. (c) Top view of the flipped CMOS chip stacked above the GIPD chip. (d) Side view of the flipped CMOS chip stacked above the GIPD chip.

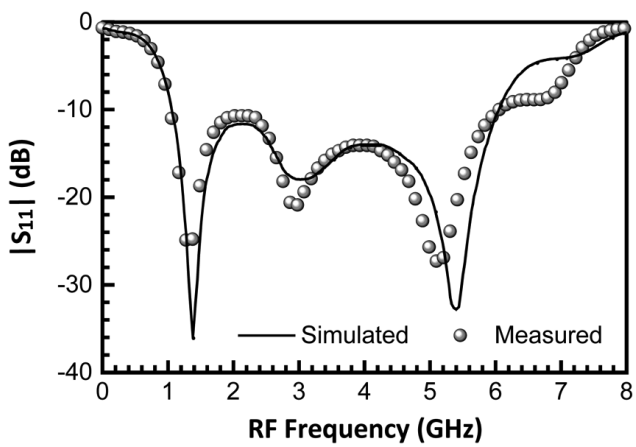


Fig. 18. Simulated and measured $|S_{11}|$ of the stacked RFE package.

of CMOS substrate leakage results in a high LO-to-RF isolation. Fig. 20 plots the simulated and measured conversion gain and NF of the stacked RFE package. Measurement results show a conversion gain of 23–25 dB and an NF of 2.2–2.8 dB within 1–6 GHz. Fig. 21 illustrates the simulated and measured IIP_2 and IIP_3 of the stacked RFE package with a two-tone spacing of 30 MHz. Measurement results further show an IIP_2 of 57–68 dBm and an IIP_3 from −5.2 to −3.5 dBm, in which the IIP_2 degradation at higher frequencies is attributed to the CMRR drop of the GIPD balun. Notably, the IIP_2 was also found degraded at larger two-tone spacing due to the reduced

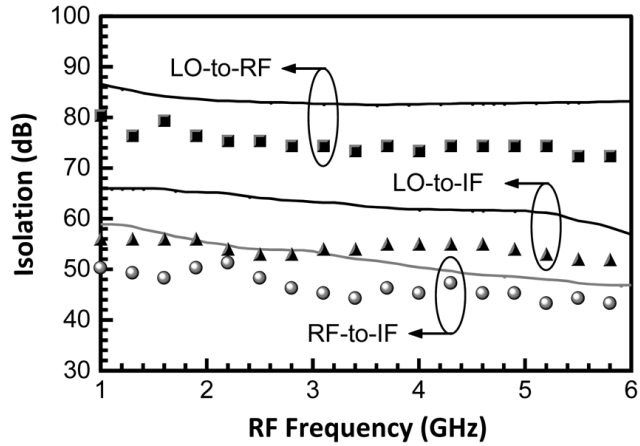


Fig. 19. Measured port-to-port isolation of the stacked RFE package. Solid lines denote simulated results, and symbols (square, triangle, and circle) denote measured results.

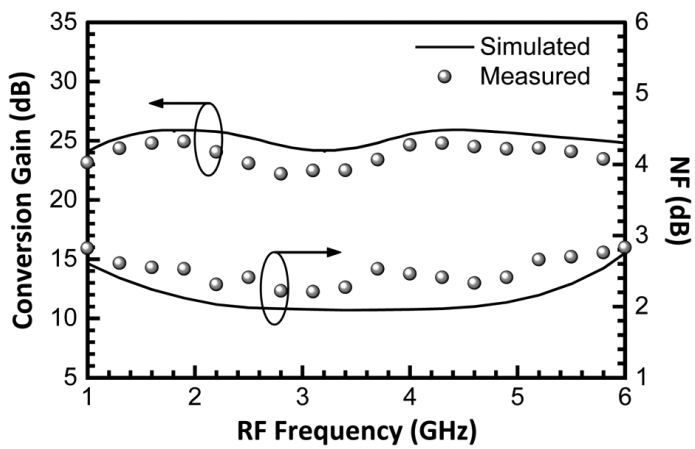


Fig. 20. Simulated and measured conversion gain and NF of the stacked RFE package.

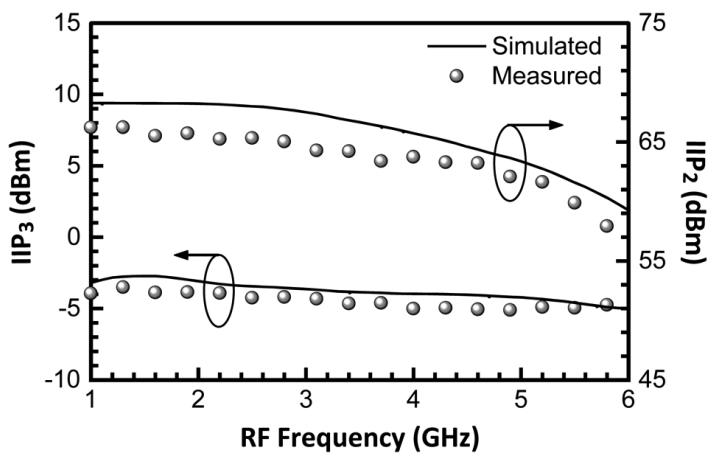


Fig. 21. Simulated and measured IIP_2 and IIP_3 of the stacked RFE package.

blocking capability of the ac-coupling capacitor between the LNA and mixer. A good agreement between the simulation and measurement results confirms the reliability of the proposed design and co-simulation procedure for a wideband CMOS RFE stacked with GIPDs.

TABLE I
PERFORMANCE COMPARISON OF THIS WORK WITH THE STATE-OF-THE-ART WIDEBAND CMOS RFEs

Reference	Frequency (GHz)	Gain (dB)	NF (dB)	IIP_2 (dBm)	IIP_3 (dBm)	Power (mW)	CMOS (nm)
This work	1 – 6	23 – 25	2.2 – 2.8	57 – 68	-5.2 – -3.5	18	180
[6]	0.6 – 10	10.5 – 14.5 *	6 – 7.5 *	21 – 28	0 – 1 *	90 [a]	45
[28]	2 – 8	20 – 23 *	4.5	18 **	-7 **	51 [b]	65
[29]	0.8 – 5	36	5	46 – 65	-3.5 **	28.5 [c]	90
[30]	3.1 – 10.6	19.5 – 21.7	3 – 3.8	20.6 – 22.3	-9.6 – -7.4	10.8 [d]	65
[3]	0.5 – 9	28 – 31	6 – 9 *	N/A	-12 – -8.3 *	54 [e]	65
[31]	0.6 – 3	42 – 48	3	N/A	-14 **	30 [a]	130

* graphically estimated; ** measured at single frequency.
[a]: including LNA, I/Q mixer, LO driver, frequency divider (FD), and transimpedance amplifier (TIA).
[b]: including LNA, single mixer, LO driver, and TIA.
[c]: only estimating LNA and I/Q mixer.
[d]: including LNA and single mixer.
[e]: including LNA, I/Q mixer, LO driver, and FD.

Table I summarizes the performance merits of this work, along with a comparison made with the state-of-the-art wideband CMOS RFEs [3], [6], [28]–[31]. The comparison reveals that this work achieves the lowest NF as well as superior IIP_2 and IIP_3 with comparable power consumption among the other RFEs. This is primarily due to the use of high-Q GIPD inductors in the LNA and the low-loss GIPD balun with a high CMRR in between the LNA and mixer. Moreover, the proposed silicon-on-glass solution is smaller in area and cheaper in cost than the full CMOS one. This is because the stacked chip structure greatly reduces the overall occupied area as well as the required CMOS chip area. Furthermore, this work uses the inferior CMOS technology to achieve superior or comparable performance to the others that use advanced CMOS technology. The cost advantage of the proposed solution is more obvious accordingly. Although in this solution the flipped CMOS chip requires some extra bumps to connect the GIPD balun and inductors, it is not a problem because the flip-chip technology involves a redistribution layer process to achieve a high bump density in providing a large number of interconnections.

V. CONCLUSION

This work demonstrates a stacked RFE package based on combined CMOS and GIPD technology. It uses high-Q GIPDs to overcome the disadvantages of low-Q integrated passive components in CMOS technology, and thus improves the RF performance of the proposed receiver RFE, resulting in an NF of 2.2–2.8 dB, an IIP_2 of 57–68 dBm, and an IIP_3 from -5.2 to -3.5 dBm over 1–6 GHz. While taking into account the post-layout parasitics of the stacked RFE package in the chip-package co-simulation, the simulation results show a satisfactory correlation with the measurement data. This correlation confirms that the proposed stacked RFE package design can properly consider the coupling effects between the flipped CMOS chip and GIPDs.

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