Full Chip-Package-Board Co-design of Broadband QFN Bonding Transition Using Backside via and Defected Ground Structure

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Abstract—A complete chip-package-board co-design of bonding transition for a quad flat pack nonlead (QFN) package was conducted from dc to millimeter wave frequencies. First, two ground paths in parallel were used to improve the operating frequency of the commercially available QFN to 50 GHz. Owing to its rectangular cross section, ribbon bond has a better form factor than the corresponding round wire bond with the same dc resistance; it is therefore more effective in impedance matching, and can carry more current at high frequencies. Ribbon bonds were utilized to improve incrementally the frequency performance. Applying the -1.5-dB rule for $|S_{21}|$ and the -10-dB rule for $|S_{11}|$, improvements are found to be 1.7 and 3.2 GHz, respectively. Second, QFN frequency performance was significantly improved by using an embedded DGS on the PCB. At 50 GHz, the transition was found to be excessively capacitive. A high-impedance DGS, being inductive itself, was used to compensate for the capacitive nature of the transition. The lumped element approach was taken to provide the background rationale how a DGS on the PCB ground can be adequately used to reduce the capacitive nature of the transition around 50 GHz. Indeed, from simulation at 50 GHz, utilizing the DGS helped to improve the impedance matching, and reduce the insertion loss, further extending the range of operating frequencies. Later, a full wave simulation of the DGS-compensated transition was conducted and the transition was experimentally validated. The full-wave simulated and experimentally obtained results are in good match. From measurements, when the DGS is used, the -1.5-dB rule for $|S_{21}|$ and the -10-dB rule for $|S_{11}|$ enable the QFN package to achieve the bandwidth up to 62.3 and 66 GHz, respectively.

Index Terms—Broadband quad flat pack nonlead (QFN) package, compensation, defected ground structure (DGS), millimeter-wave package, ribbon bond interconnect.

I. INTRODUCTION

THE ever increasing needs for broader frequency bandwidth driven by the strong growth of data communications have pushed devices into microwave, millimeter-wave, and optoelectronics bands [1], [2]. For this reason, the selection of a package is critical, because the IC-package interconnects can directly influence the overall system performance. Minimizing any impedance mismatch that is associated with the IC-package interconnects for a wide frequency band such that the final product will meet the performance, is a challenge. In addition, it is important to rein in the package costs. One way to achieve this is to apply the most frequently used package for high frequencies. For example, the quad flat pack nonlead (QFN) package has been widely used for RF ICs owing to its simple, low parasitic design.

Conventionally, wire bonding has been the most popular first-level interconnection choice. Although wire bonding is reliable and cost-effective, it cannot be utilized in millimeter-wave applications, because it is mostly ineffective at frequencies above 20 GHz [3]–[5], owing to the impedance mismatch from the self-inductance of the bonding wires and the shunt capacitance from the pads and molding. Although there are some approaches that have been shown to perform adequately up to 60 GHz, these, however, require substantial modifications of the conventional, cost effective solutions. For example, in the approach [6], impedance matching requires a large area and because of the lack of molding protection, it does not represent a final package solution. In [7], extensive tooling cost was required. In [8], the frequency response is satisfactory only in narrow 60-GHz band applications. In our previous work [9], two ground paths in parallel to minimize the signal inductance at the IC-to-package interface to achieve broadband matching without the need for any additional matching network, but this approach only extended the operating frequency to 50 GHz.

Continuing to improve the performance, ribbon bond, instead of round wire bond, was used in another report [10]. The two attractive properties of the ribbon bond are its higher capacitance, which makes it more effective in impedance matching since wire bonds are intrinsically inductive, and its resistance to skin effect since the currents penetrate deeper at the corners of the ribbon bond [11]–[13]. These advantages support better impedance match at the IC-package interface [14]. However, the ribbon bonding alone is not enough to support our applications at frequencies greater than 60 GHz. It is because the impedance mismatch between the QFN package and the PCB carrier interface at 50 GHz is quite pronounced, and the plastic molding materials are quite lossy [15].
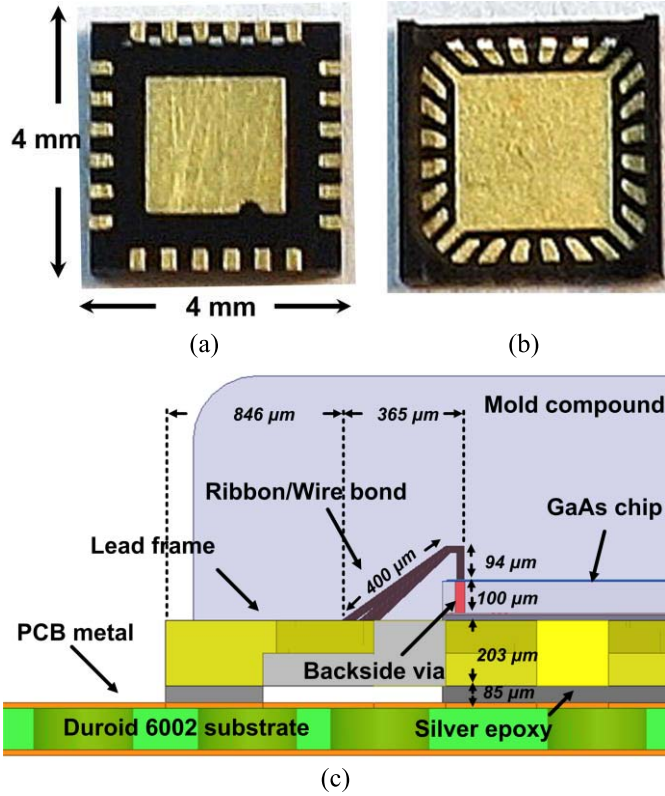
Fig. 1.   QFN package structure. (a) Bottom view. (b) Top view before encapsulation. (c) Side view of the package after encapsulation.

In this paper, Section II presents the above results concerning the use of two ground paths in parallel and ribbon bonds, which extend the frequency range to 50 GHz. Then, for the first time, a defected ground structure (DGS) is adopted to compensate for the intensive capacitive nature of the IC to QFN transition at frequency range near 50 GHz. The effectiveness of DGS in reducing the impedance mismatch at the package to PCB interface is shown in Section III. The immediate result of this DGS compensation is to extend the frequency range to 60 GHz or above.

II. CHIP-PACKAGE TRANSITION DESIGN USING BACKSIDE VIAS AND RIBBON BONDS

A. QFN Package With a Plastic Molding Compound

The conventional 24-pin QFN package, shown in Fig. 1(a) and (b), is relatively inexpensive and widely used in electronics industry. Fig. 1(c) shows a side view of this package. A GaAs chip was attached to a QFN die paddle using silver epoxy. The QFN was then attached to Duroid 6002 substrate using silver epoxy. The die bond pads were ribbon-bonded or wire-bonded to the metal leads of the QFN package; the assembly was encapsulated with a plastic molding compound. The metal lead pitch was 0.5 mm. In addition, the plastic molding compound had a higher dielectric constant (ε_r) and a greater loss tangent than air. The compound protected the IC and wire bonding; the effects of the encapsulating material must be included in any accurate determination of circuit performance. Here, a dielectric constant of 4.8 and loss tangent of 0.02 were chosen for

the mold compound. In Fig. 1(c), backside vias (BSVs) are shown. The vias are commonly employed to dissipate heat and reduce ground inductance for the GaAs IC. Indeed, GaAs is not an ideal heat sinking material.

B. Two Ground Paths in Parallel

As previously mentioned, package performance at mm-wave frequencies is of particular interest. The performance bottlenecks are the conductor or dielectric losses and the inductive nature of signal and ground paths. Therefore, a good RF ground path is an essential part of a well-designed microwave circuit. In this paragraph, two ground paths in parallel were utilized herein to reduce overall inductance by creating the second path through the BSV. The paths were accomplished by bonding either a round wire or ribbon wire on the BSV at both ground paths, G_1 in Fig. 2(a). In [9], it was shown the second path had helped to extend the package operating frequency up to 50 GHz. This improvement was due mainly to the decrease in inductance achieved by the dual ground path. Here, we show how the dual ground path had resulted in a lower overall inductance reducing the mutual inductance. Consider the two ground paths are in proximity to each other and the currents flow in the same direction; the effective inductance is obtained by [16]

$$L_{\text{eff}} = \frac{L_1 L_2 - L_M^2}{L_1 + L_2 - 2L_M} \tag{1}$$

where L_1 and L_2 are the inductance of loops S_1–G_1 and S_1–G_2, respectively. L_M denotes the mutual inductance between the two loops. In (1), L_{eff} and L_2 are obtained empirically: L_{eff} is obtained by de-embedding the electrical characteristics of the transition with both G_1 and G_2 paths present; L_2 is obtained by de-embedding the electrical characteristics of the transition without the G_1 path. The key to the dual ground path design is that the effective inductance, L_{eff}, must be smaller than L_2, the inductance of the original ground path. Indeed, L_{eff} and L_2 were measured to be 0.43 and 0.7 nH, respectively. L_1 cannot be independently obtained from measurements, since the original ground path G_2 is always present. However, based on the dual path configuration that is shown in Fig. 2(a), L_1 and L_2 can be safely assumed to be equal, since the two paths were designed to be about the same length. Using the measured inductance of L_{eff} and L_2, we were able to obtain a coupling coefficient k of 0.2 from (1), where $k = L_M/\sqrt{L_1 L_2}$. This value indicates that the dual ground path design is in a right design space, since a higher k would results in a L_{eff} with the same magnitude as L_1 or L_2, which is against the purpose of obtaining a lower effective inductance at the transition.

The above result can be validated by plotting k versus the opening angle (θ) of the two loops, S_1–G_1 and S_1–G_2, as shown in Fig. 2(a). Based on the structure of Fig. 2(a), two identical loops, as shown in Fig. 2(b), were formed and the coupling coefficient k was simulated as a function of θ. For a k of 0.2, θ is about 30°. The dimensions in Fig. 1(c) were used to estimate a θ of 29°, validating our design. Although k decreases as θ increased, as shown in Fig. 2(b), the self inductance of the two loops is also effectively increased
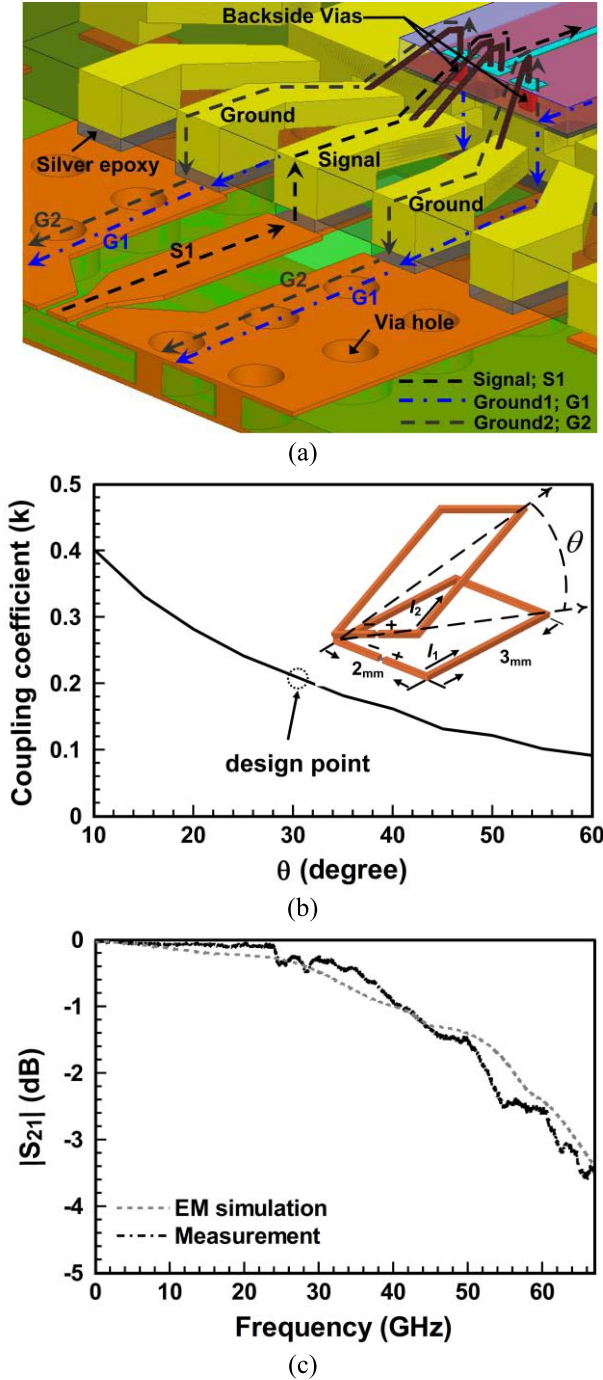
(a)

(b)

(c)

Fig. 2. Two ground paths in parallel. (a) Signal and ground flow between the PCB and GaAs chip through the coplanar wirebond interconnect. (b) Coupling coefficient varying with the angle θ between two rectangular loops open diagonally. (c) Comparison of EM simulated and measured insertion loss.

with the angle because of the height and length of the wire bond. Therefore, in the best design, the open angle is in the region from 28° to 32°.

The characteristic of the QFN transition employing the dual ground paths design is shown in Fig. 2(c). From the simulation and the very carefully executed conductor backed coplanar waveguide (CB-CPW) for wideband signal propagation design, chip to package and package to board mount flatness with silver epoxy and de-embedding accuracy for our
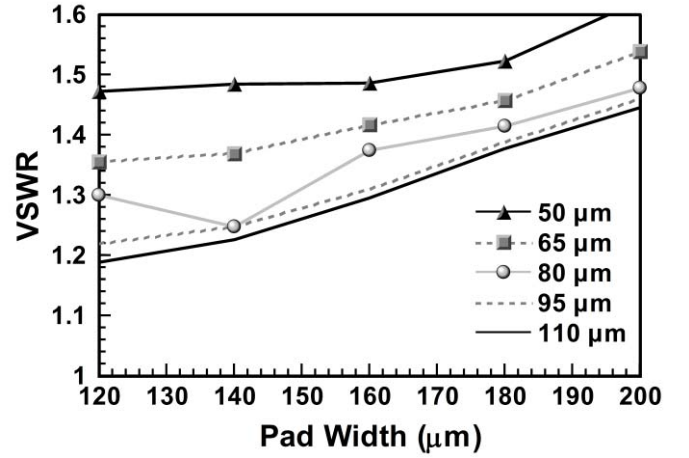

Fig. 3. Simulated VSWR as a function of GaAs pad width for different ribbon bond widths.

experimental validation. Finally, the QFN has a 1.5 dB for insertion loss and the transition design reached an operating frequency of 50 GHz.

C. Performance Comparison of Various Configurations of Ribbon Bonds and Wire Bonds

In Section II-B, the two ground paths in parallel were helpful in pushing the operating frequency to 50 GHz. In this section, various interconnection schemes that involve round and ribbon bond wires are analyzed. Here, ribbon bonds are a bonding structure of rectangular cross section. Therefore, the thickness and width of ribbon bonds can be independently chosen. Because of the flat portion and the two corners, the ribbon bonds have larger distributed capacitance. Consequently, it is easier for a designer to obtain matched impedance using ribbon bonds. A higher return loss is desirable as it results in a lower insertion loss. Notably, a round wire is intrinsically an inductor since its capacitance is very small.

Fig. 3 shows the VSWR for various ribbon bond transitions. Let the reflection coefficient be Γ, the VSWR is given by the following formula:

$$\text{VSWR} = \frac{1 + \Gamma}{1 - \Gamma}. \tag{2}$$

The width of the ribbon in the transitions should be chosen such that the VSWR is as small as possible to avoid any discontinuity, and to minimize the reflection at the transition. A wider ribbon width can result in a lower VSWR; however, it would require a larger pad width. A larger IC pad would results in a larger parasitic capacitance, larger signal leakages, and impedance mismatching at higher frequencies. Therefore, based on the simulation results as shown in Fig. 3, a ribbon width of 75 μm and a thickness of 15 μm are chosen, and the chip pad width is set to 140 μm, yielding a VSWR of 1.28. Another advantage of ribbon bonds is that the ribbon bonds exhibit resistance to the rapid increase in ac resistance increase that is caused by the skin effect. It is because of the existence of the low density currents at the corners of the ribbon bonds. In [10], it shows that the ribbon bond indeed exhibited less ac resistance compared with that of a round wire which has the same dc resistance. This phenomenon helps
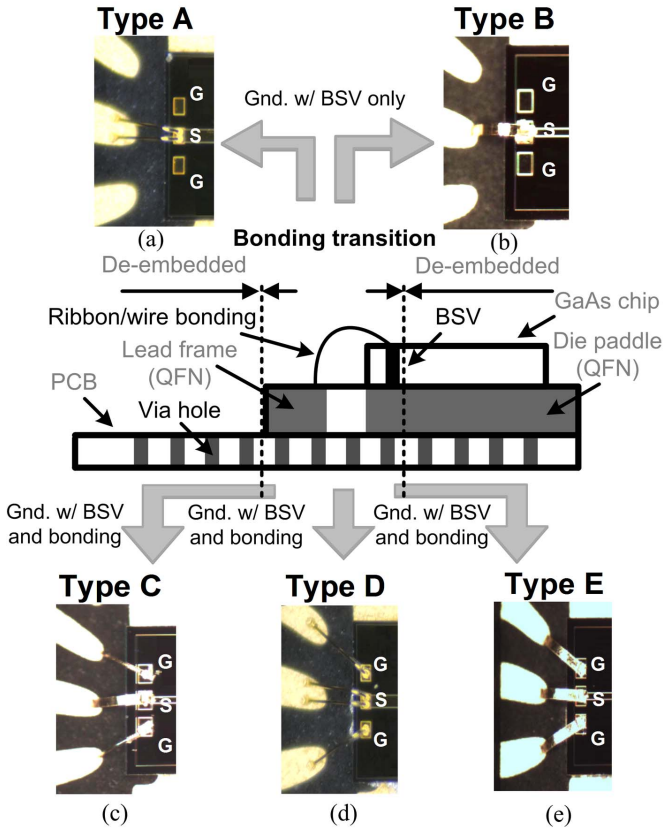
Fig. 4. Photographs of five different types of bonding. (a) Type A: two round wires in parallel on the signal pad. (b) Type B: single ribbon bond on the signal pad. (c) Type C: a round wire on each ground pad and a gold ribbon bond on the signal pad (ribbon length = 465 μm). (d) Type D: a round wire on each ground pad, two round wires in parallel on the signal pad (length = 375 μm). (e) Type E: a ribbon bond on ground and signal pads (length = 465 μm). All ribbon and round wires were made of Au.

to reduce the insertion loss of the interconnection scheme using ribbon bonds. In the following paragraphs, we will demonstrate the effectiveness of ribbon bonds in extending the operating frequency.

Fig. 4 shows the photographs of five interconnection schemes for QFN packaged GaAs chips. Two of these schemes (Types A and B) have a single ground path S_1–G_2; the remaining three (Types C, D, and E) have dual ground paths. Detailed description of the interconnection schemes, such as material, bonding type, and dimensions, is also given at the caption for Fig. 4. Measured insertion loss results are shown in Fig. 5. Using the criteria of $|S_{11}| = -10$ dB, and $|S_{21}| = -1.5$ dB, the valid operating frequency range of different interconnection schemes is summarized in Table I. Types A and B clearly reveal the reduction of insertion loss by the ribbon. Furthermore, a comparison of Types B and C clearly reveals the effectiveness of the dual ground path in extending the operating frequency from 40 GHz to 50 GHz. The afore-mentioned benefits of the ribbon can be obtained by comparing Type C, Types D and E.

III. DGS DESIGN

As shown in Section II, the carefully implemented ribbon bonding scheme alone is not enough to support frequencies that exceed 60 GHz. Further analysis reveals severe impedance
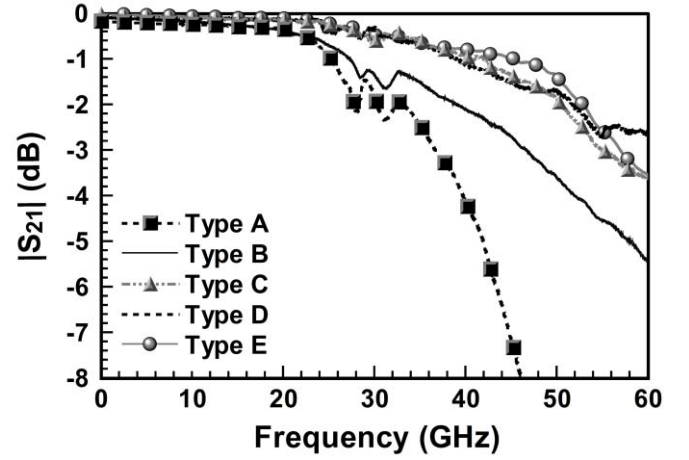

Fig. 5. Measured insertion loss results for five different types of bonding transitions.

mismatching at 50 GHz for interconnection of Type E. At this frequency, the transition turned excessively capacitive. To alleviate this mismatch, a defect ground structure, which is inductive in nature, was utilized to bring the impedance of the transition to close to 50 Ω. This strategy is essentially the same as that employed in Section II-C to improve the range of operating frequencies. In this section, lumped element models are used to explain the mechanism. The chip-package-board transition is definitely not a lumped circuit at the frequencies of interest (from dc to 60 GHz). However, the use of the lumped circuit method with input impedance Z_{in} at 50 GHz facilitates the illustration of the design. In Section IV, full-wave modeling and experiments are carried out to validate the methodology.

A. Lumped Models for Realization of a High Impedance Transition

The transition can be modeled as a section of transmission line with a characteristic impedance of Z_h and an electrical length of θ_h. At lower frequencies, the transition, being a small part of the wavelength, can be modeled as a lumped element. From Fig. 6, a section of transmission line can be represented as a lumped T model circuit. The inductance and capacitance can be obtained from [17]

$$L = \left[\frac{2Z_h}{\sin \theta_h} (1 - \cos \theta_h) \right] \Big/ \omega \quad (H) \qquad (3)$$

$$C = \left[\frac{1}{Z_h} \sin \theta_h \right] \Big/ \omega \quad (F) \qquad (4)$$

where ω is the angular frequency. Equations (3) and (4) indicate that inductance increases with characteristic impedance. To obtain an inductive section, it is important to get a section with a high Z_h. From S-parameter measurement, Z_h and θ_h can be obtained from the Z, Y, and S matrices of the element, as follows:

$$Z_h = \sqrt{\frac{\text{imag}(Z_{11})}{\text{imag}(Y_{11})}} \qquad (5)$$

$$\theta_h = \tan^{-1} \left(-\frac{\tan \theta_{21}}{A} \right) + n\pi \qquad (6)$$

TABLE I
MEASURED PERFORMANCE SUMMARY FOR DIFFERENT BONDING TRANSITIONS

	Type A	Type B	Type C	Type D	Type E
*BW$|s_{11}|$ (GHz)	31.1	37.1	49.8	50	53
*BW$|s_{21}|$ (GHz)	27.3	35	50.1	50.3	51.8

* Criteria used: $|S_{11}|$ = -10 dB for BW$|s_{11}|$; $|S_{21}|$ = -1.5 dB for BW$|s_{21}|$. Unit: GHz
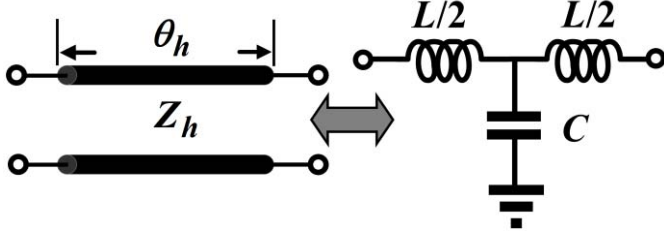

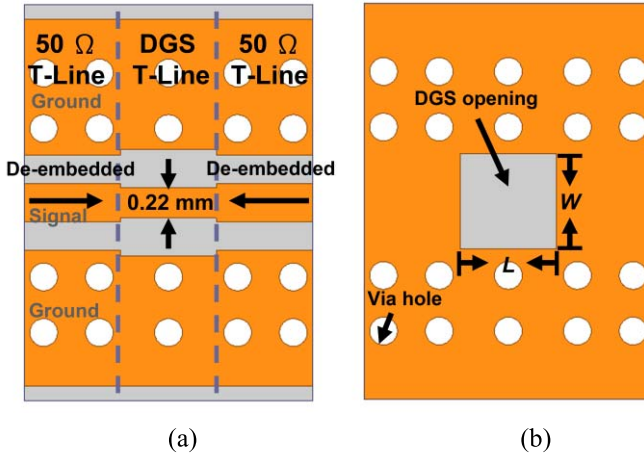Fig. 6.   Schematic of a conventional transmission line and its T model.

Fig. 8.   Post-layout EM simulation of DGS characteristic impedance with different W.

Fig. 7.   DGS configuration. (a) Top view. (b) Bottom view.

where θ_{21} is the angle of S_{21}. Z_{11}, Y_{11}, and S_{21} are the elements of matrices Z, Y, and S. $A = (50/Z_h + Z_h/50)/2$, and n is an integer of 0, 1, or 2.

An inductive section can be realized in two ways: one is through a section of narrower signal line; the other is through a DGS on the ground. Fig. 7 shows the top and bottom views of the physical layout for the section that contains both. A line width of 0.22 mm was chosen so the specific section exhibits a characteristic impedance of 60 Ω without any DGS on the ground.

The characteristic impedance of the transition can be increased by increasing the width of the DGS openings, as shown in Fig. 8. However, the width cannot exceed 0.7 mm, owing to limitations on the placement of the ground vias. In the following analysis, the signal line was not narrowed since the signal line was fixed by the package lead; hence, DGS opening becomes the only choice to implement a high-impedance section efficiently.

B. Optimization of Transition by Impedance Matching

Fig. 9(a) shows a 3-D chip-package-board transition in which the GaAs chip was bonded by gold ribbons on the
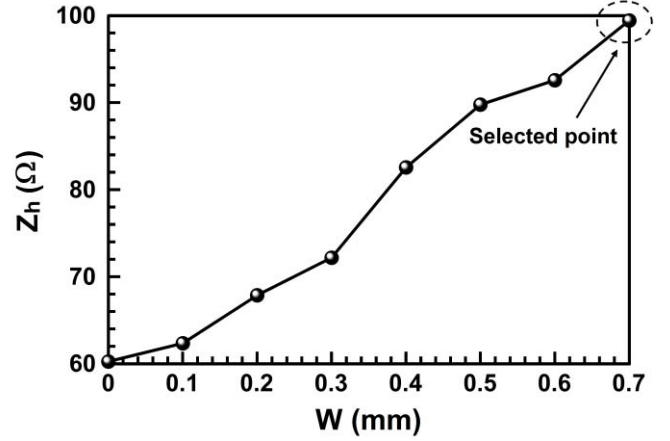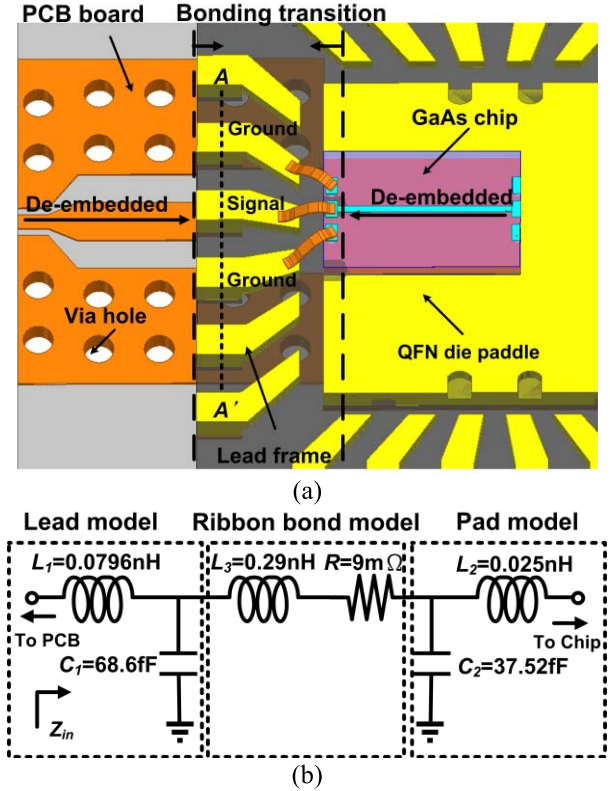

Fig. 9.   Chip-to-package-to-board illustration. (a) QFN on board without DGS configuration. (b) Equivalent π model of bonding transition at 50 GHz.

pads, and attached to a commercial 4-mm × 4-mm QFN package using silver epoxy. The microstrip line on the GaAs chip was co-designed with presence of the plastic molding
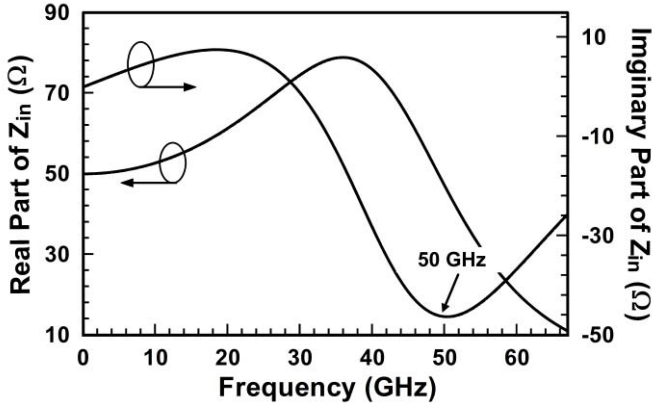
Fig. 10. Input impedance of QFN package transition without a DGS from EM simulation.

material to be 50 Ω. At the PCB side, the transition can be considered as a conductor backed coplanar waveguide (CB-CPW), owing to the presence of the PCB ground. Both the microstrip and the CB-CPW should be designed to be as close to 50 Ω as possible, facilitating de-embedding, and increasing the accuracy of the results. After the microstrip line on the chip and CB-CPW on the PCB board were de-embedded, the characteristics of the transition were obtained [18], [19].

An equivalent π model of the transition without a DGS was created and is shown in Fig. 9(b). The frequency for the model was extracted to be around 50 GHz. The impedance plot looking into the equivalent π model, Z_{in}, is shown in Fig. 10. From the imaginary part of Z_{in}, the transition becomes capacitive after 30 GHz with the lowest point at 50 GHz. Notably, that since the transition becomes distributive at high frequencies, Z_{in} approach, instead of Z_h, was taken. Using Z_{in}, the overall broadband effects are known.

With the help of Ansys HFSS, Fig. 11(a) and (b) shows the magnitude of the electric field at the transition along $A–A'$ without and with a DGS, respectively, at 50 GHz. Clearly, the propagation mode without a DGS has turned from a CB-CPW mode to a microstrip mode at the PCB end, as shown in Fig. 11(a). Previously, Z_{in} was found to be excessively capacitive at the same frequency. In contrast, Fig. 11(b) plots the electric field along the $A–A'$ line for a DGS-compensated transition at 50 GHz; it shows a CPW propagation mode. Circuit modeling similar to that associated with Fig. 9(b) was performed for this DGS compensated transition. Surprisingly, the capacitance C_1 was almost unchanged. That is, the mode change did not result in the excessive capacitance. The larger leads may be the underlying cause of the excessive capacitance. The only change was an increase in L_1 by 0.07 nH, from the original 0.08 nH, which can be accounted for by the embedded DGS.

Fabricating a DGS right under the transition represents a challenge to model it accurately. It is because the previously obtained transition model [i.e., Fig. 9(b)] would automatically become invalid once a DGS under the transition is added. However, if only the electrical property at 50 GHz is considered, then the DGS-compensated transition Z_{in} can
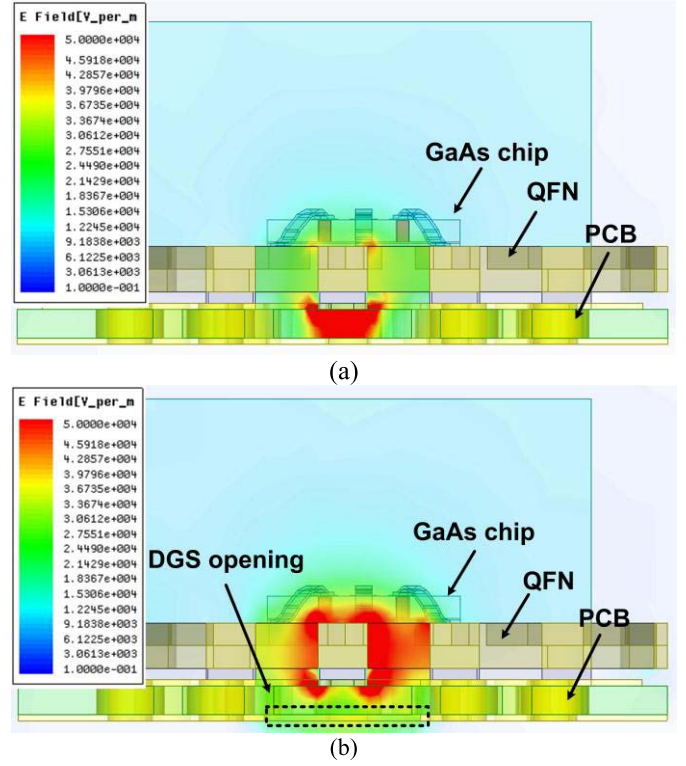

(a)

(b)

Fig. 11. Electric field magnitudes along $A–A'$ for Fig. 9(a) at 50 GHz. (a) Without a DGS. (b) With a DGS.
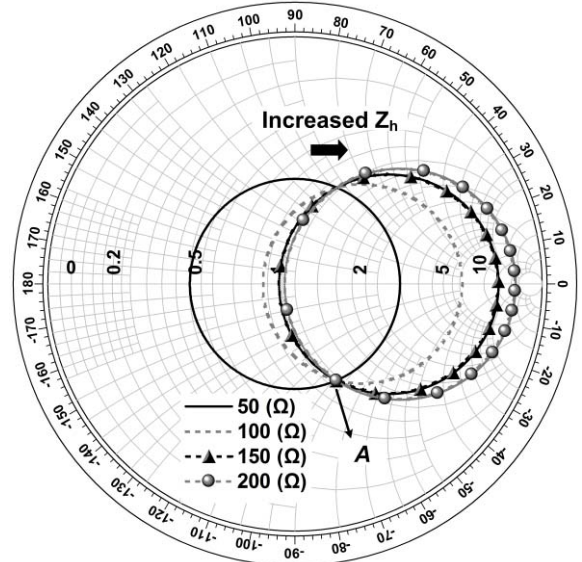

Fig. 12. Loci of S_{11} of the combined circuit with varied characteristic impedances of the lumped DGS section.

be obtained by connecting the original $Z_{in} = 50 * (0.946 − j0.938)$ Ω with a lumped DGS model (assuming a short electrical length of, for example, less than 30°) to the left. Based on the transmission line model, the combined circuit represents a model for the DGS compensated transition. In the transmission line, the DGS effect is accounted for in the signal line.

Fig. 12 pots the loci of S_{11} of the combined circuit with varied characteristic impedances of the DGS section. As the characteristic impedance is increased, the locus is moved toward right. By altering the length of the DGS section at
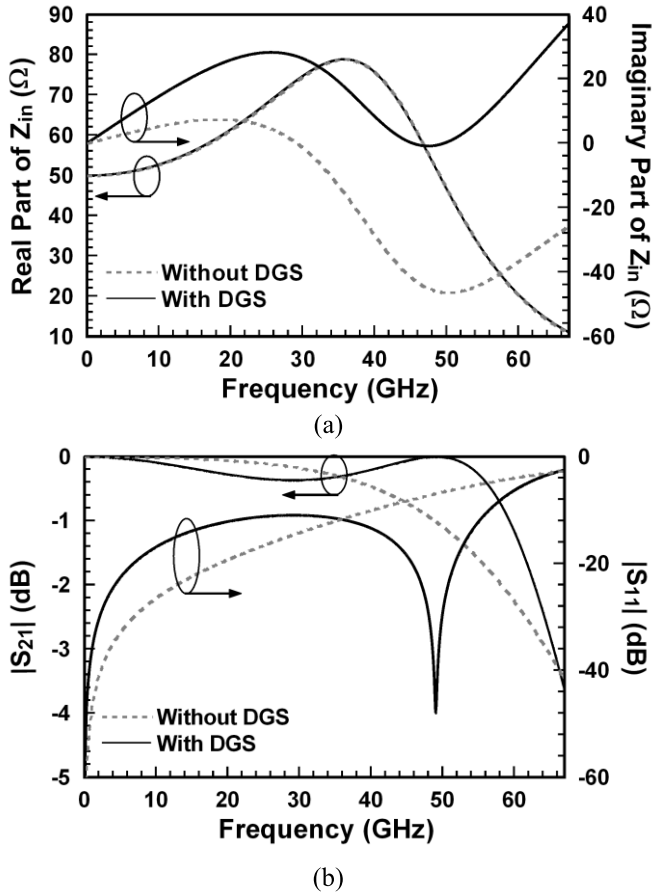
Fig. 13. Simulation results of the chip-to-package-to-board transition for $Z_h = 200$ Ω. (a) Real and imaginary of Z_{in} for original and DGS compensated transitions. (b) Extracted S-parameters for the transitions.

a characteristic impedance of 200 Ω, it would be possible to achieve a perfect match (i.e., bringing from point A to the 50-Ω center).

Fig. 13(a) shows the real and the imaginary parts of Z_{in} of the original and the DGS embedded transitions. Clearly shown in the figure is the less capacitive imaginary part of Z_{in} for the DGS embedded transition at 50 GHz. Also noted is the fact that the real parts remained the same.

Using the Agilent circuit simulation tool ADS, S-parameters for the original and the DGS embedded transitions are obtained. The length of the DGS in the simulation was 21° at 50 GHz, and a characteristic impedance of 200 Ω was picked. The insertion loss of the transition without the DGS drops dramatically after 30 GHz as shown in Fig. 13(b). On the contrary, the insertion loss of the DGS-compensated transition has improved drastically. At 50 GHz, S_{21} is at a maximum in magnitude, owing to a perfect match at 50 GHz. From Fig. 13(b), optimization of the insertion loss S_{21} at 50 GHz extended the overall bandwidth from less than 50 to 60 GHz when the −1.5-dB rule for $|S_{21}|$ was adopted.

In this DGS section, the lumped approach using $Z_{in} = 50*(0.946 - j0.938)$ Ω, and a section of electrically short (at 50 GHz) DGS is taken. Owing to improved impedance matching, S_{21} was optimized at 50 GHz, causing the overall operation bandwidth to reach over 60 GHz.
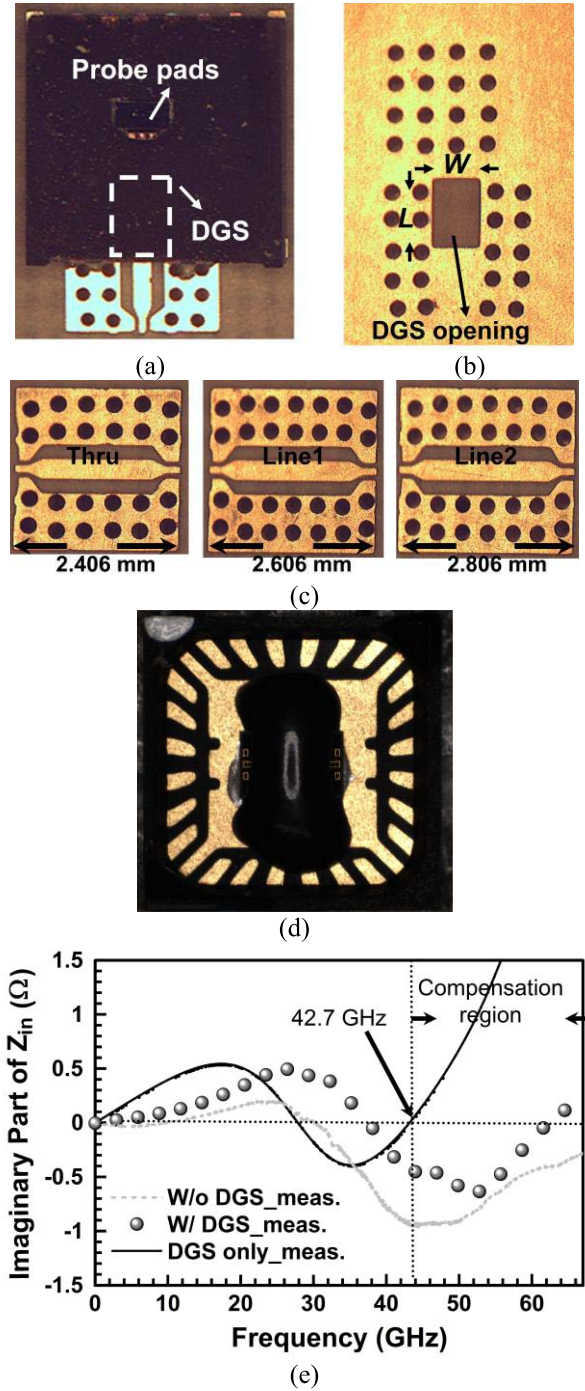

Fig. 14. (a) Top view of the QFN package on board and with DGS. (b) Bottom view shows the DGS. (c) Photograph of the TLL de-embedding kits. (d) Photograph of the GaAs chip with plastic molding. (e) Imaginary part of Z_{in}, DGS is shown to compensate by inductive to the transition after 42.7 GHz.

In reality, the original and the DGS embedded transitions are not lumped circuits. In Section IV, full-wave modeling and experiments are conducted to validate this methodology.

IV. MEASUREMENT RESULTS AND DISCUSSION

A QFN, attached to a board with a DGS, as shown in Fig. 14(a), was fabricated and measured. Under the white dotted rectangle in Fig. 14(a) lies the DGS-compensated transition. Fig. 14(b) shows the bottom view of the transition,

where a DGS opening with L and W is clearly depicted. The actual width of the DGS, was chosen to be 0.7 mm, which corresponds to $Z_h = 100$ Ω as shown in Fig. 8. The QFN lead actually determines the width of the signal line at the transition above the board.

S-parameter measurements were made in the frequency range 0.1–67 GHz using an Agilent N5247A PNA-X network analyzer. To obtain precise values of the bonding transition S-parameter, the traces on PCB and the GaAs chip, as shown in Fig. 9(a), need to be de-embedded. The thru-line-line (TLL) calibration technique [20] was applied for this purpose. Fig. 14(c) shows the de-embedding kit structures. The characteristics of the transition with and without DGS are shown in Fig. 14(e). Obviously, the ribbon bond circuit without DGS is shown to turn capacitive from inductive at 30 GHz. As explained earlier, the elongated return ground paths of the DGS opening would help to turn the transition more inductive, as be seen from the DGS only plot (solid line) in Fig. 14(e). Therefore, adding the inductive DGS to the ribbon bonding transitional structure significantly reduced the capacitance at and above 42.7 GHz. The imaginary part of Z_{in} for the circuit is also shown in Fig. 14(e), the line with round circles.

In Fig. 15(a), the measurement results of $|S_{21}|$ and $|S_{11}|$ with and without the DGS opening are shown. Specifically, $|S_{11}|$ with the DGS exhibits impedance matching up to 66 GHz if a return loss of 10 dB is used. As a result, $|S_{21}|$ with the DGS extended the 1.5-dB insertion loss to 62.3 GHz, while $|S_{21}|$ without DGS only reached 50.4 GHz. This translates to an extension of 11.9 GHz in the applicable frequency band. The result is consistent with our analysis of DGS in Section III; which that, DGS supports matching at high frequencies of 50 GHz and above. In order to illustrate the performance of the proposed method, the smith chart representation of S_{11} is shown in Fig. 15(b). The dashed circle is the Gamma circle, indicating the border of $|S_{11}|$ equal to -10 dB. From the S_{11} curves, the DGS compensated transition clearly stays within the Gamma circle bound up to 66 GHz. The uncompensated transition falls outside the Gamma circle at around 42 GHz.

In addition, Fig. 15(c) shows the simulation and measurement insertion loss data for ribbon bond transition assisted with the DGS. Since in the experiment, the molding compound was applied using glob top dispensing, that molding compound might not have been as thick as in the simulation. Overall, they are in good agreement. Importantly, both $|S_{11}|$ curves started to trend down around 40–42 GHz and showed a resonance around 54–58 GHz. This resonance caused a dip in $|S_{11}|$, leading to an improvement in signal propagation in $|S_{21}|$. In particular, at around 50 GHz, both $|S_{21}|$ curves peaked before trending down, reflecting the compensatory effect of the DGS.

Finally, a few remarks are made to provide a general perspective of this work. At first, the dual ground path helped to reduce the inductance of the transition at the lower frequencies. The dual ground path was realized using BSV and a bonding wire. The result can be applied in CMOS design where through silicon vias are used.

At 50 GHz, the signal propagation mode changed at the PCB end of the original transition. From the models of the
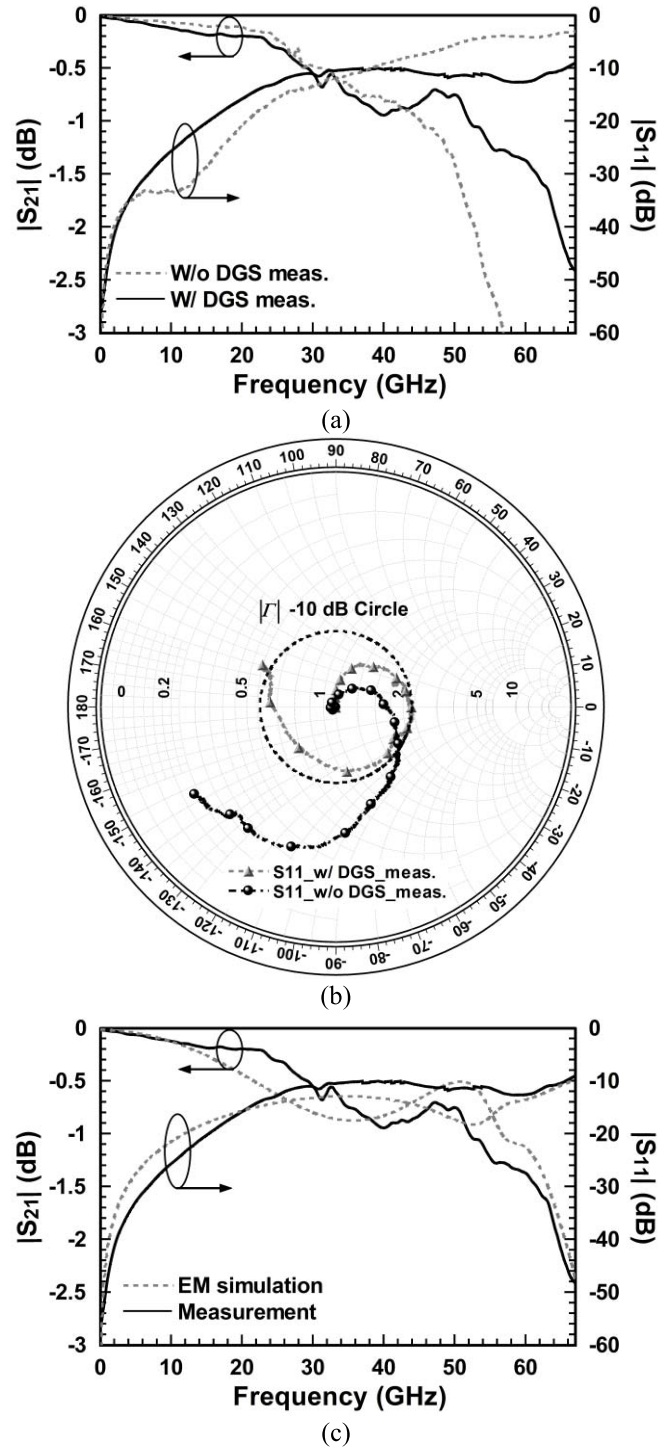

(a)

(b)

(c)

Fig. 15. Comparison of measured and simulated results of transitions with and without the DGS. (a) Measured results of $|S_{11}|$ and $|S_{21}|$. (b) Smith chart of S_{11}. (c) Simulated and measured results of $|S_{11}|$ and $|S_{21}|$ with the DGS.

original and DGS-compensated transitions, the propagation modes did not influence the capacitive loading at the PCB side. Hence, it is the inductive compensation, a direct result of the DGS opening that causes impedance matching around 50 GHz [see Fig. 14(e)].

The co-design herein accounts for the effects of the plastic molding, which is required for IC protection, have

been included. Notably, the DGS is fabricated external to the QFN, so the design of the QFN need not be altered. Only minimal care has to be taken in the design flow to institute such co-design. The proposed technique can thus be immediately applied to many other QFNs or packages with similar lead configurations.

V. Conclusion

Full chip-package-board co-design of bonding transition for a QFN package was conducted from dc to millimeter wave frequencies. During the optimization of the bonding transition, the impedance matching principle was applied to improve the overall signal propagation. First, two ground paths in parallel were used to improve the operation frequency of the commercially available QFN to 50 GHz (Type C, Table I). Because of its rectangular cross section, the ribbon bond was better able to achieve impedance matching, and carried more current at high frequencies than the corresponding round wire bond with the same dc resistance. Ribbon bonds were employed to improve incrementally the frequency performance. Applying the -1.5-dB rule for $|S_{21}|$ and -10-dB criterion for $|S_{11}|$ are used, the improvements are 1.5 and 3 dB (Types C and E, Table I), respectively.

Furthermore, for the first time, QFN frequency performance was significantly improved by using an embedded DGS on the PCB. At 50 GHz, the transition was found excessively capacitive. A high-impedance DGS, being inductive itself, was used to compensate for the capacitive nature of the transition. The DGS was fabricated directly under the transition area. At the frequencies of interest, the DGS-compensated transition behaved like a distributed line, instead of as a lumped element. In order to provide the background rationale how the DGS can be adequately employed to compensate out the capacitive nature around 50 GHz, the lumped element approach was used. Indeed, from simulation at 50 GHz, the DGS opening helped to improve impedance matching, and reduce the insertion loss; thus, further extending the range of operating frequencies. Later, full wave simulations and experiments were conducted to validate the benefits of the DGS opening. The full wave simulated and experimentally obtained results are in good match. From the measurements, employing the DGS additionally and using -1.5-dB rule for $|S_{21}|$ and -10 dB criterion for $|S_{11}|$, the QFN package is able to achieve a bandwidth up to 62.3 and 66 GHz, respectively.

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